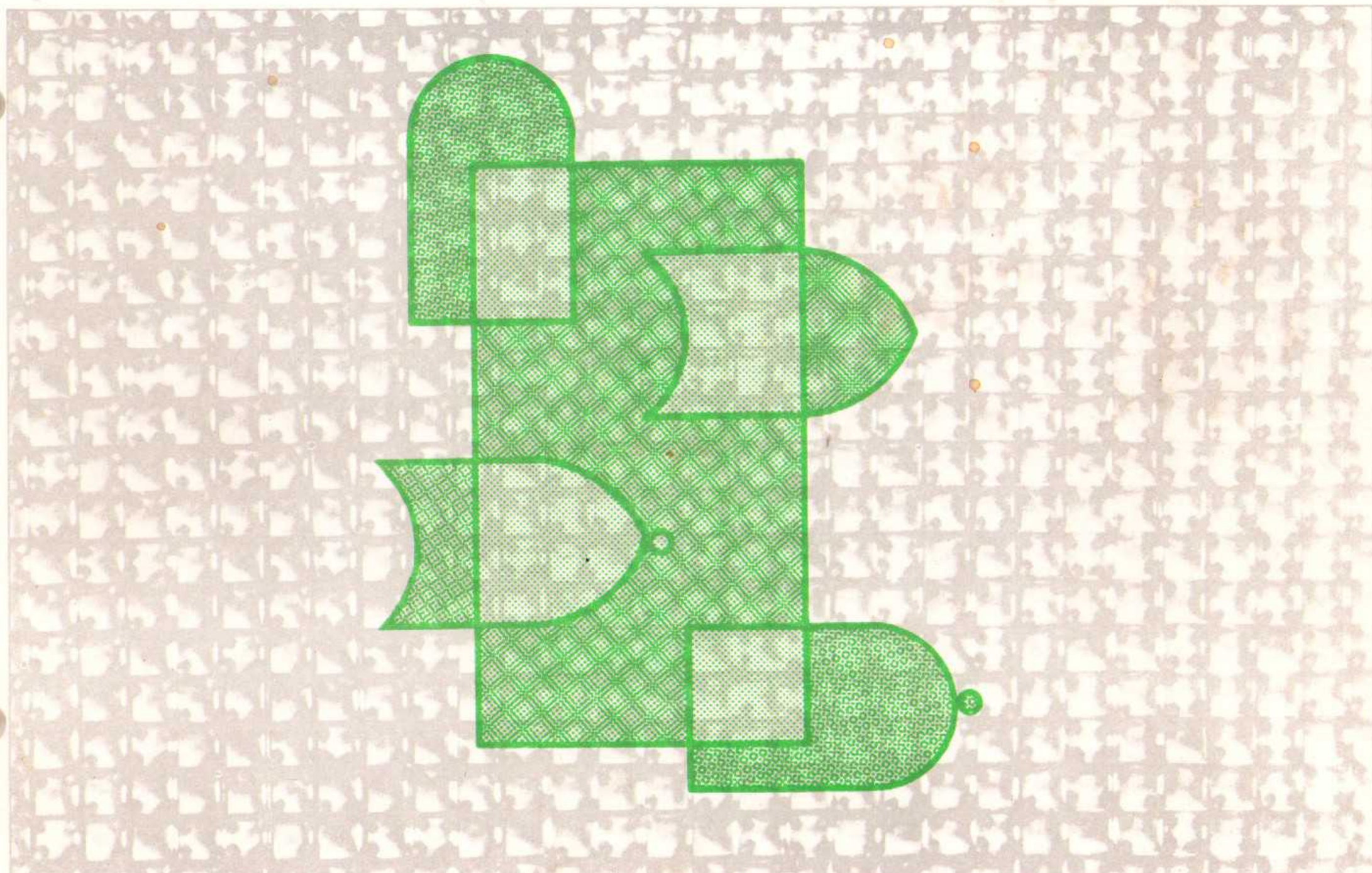
TECHNISCHE DOCUMENTATIE 1971

DEEL 1 2 3 4 5 6 7 **8** **9** **10** **11** **12**

TECHNISCHE GEGEVENS TTL GEÏNTEGREERDE SCHAKELINGEN



B.V. TECHNISCHE HANDELMAATSCHAPPIJ

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van dam ELEKTRONICA

- leverancier van hedendaagse elektronica -

Prijs als los deel f 5,00

"Technische Documentatie" is een informatie-uitgave van de B.V. Technische Handelmaatschappij Van Dam Elektronica te Rotterdam en omvat per jaargang circa 300 pagina's technische informatie over hedendaagse bij deze Handelmaatschappij verkrijgbare produkten van wereldfabrikanten. Een komplete jaargang, waarvan de verschijningsdata vrij willekeurig zullen vallen door de onregelmatige binnenkomst van bruikbare informaties, kost voor de jaargang van 1971 *f* 12,50 incl. 4% B.T.W. en voor de komende 1972 jaargang *f* 15,= incl. 4% BTW te voldoen bij vooruitbetaling per giro nummer 295550.

Verhuizingen

Verhuizingen dienen onmiddellijk na het U bekend worden aan onze administratie te worden opgegeven en niet op de dag dat U verhuist: een vroegtijdige adresverandering voorkomt vertraging en hoge extra kosten in het ontvangen van Uw documentatie!

Inleiding

Lang gewacht, toch nog uitgekomen ..... Dit zou U wellicht bij het openslaan van deze pagina hebben verzucht. Een reaktie, waarover wij echter niet verwonderd zijn en slechts vermelden, dat deze documentatie geen maandblad voorstelt doch een informatie-uitgave van ons bedrijf. Door de inventarisatie en verhuizing in begin januari is de vertraging iets verder uitgegroeid dan tot dusverre gebruikelijk was. Ook de enorme toename van ons relatiebestand is hiervan een oorzaak geweest.

VOOR 1972 is een voortzetting van het abonnement mogelijk tegen een betaling van *f* 15,= per jaar, wederom bestaande uit ca. 300 pagina's informatie en incl. 4% B.T.W.. Deze uitgave wordt gepresenteerd als kwartaalnummer en zal omstreeks de Fiarex bestaan uit een uitgebreid programma-overzicht betreffende ons totale leveringsprogramma. Losse kwartaalnummers zullen *f* 5,= per deel kosten. In de 5-de jaargang worden tevens uitgebreide tabellen opgenomen betreffend ons halfgeleiderprogramma en bouwbeschrijvingen van onze versterkers. Verlengt U Uw abonnement op tijd met de separaat toe te zenden acceptgirokaart: deze bevat alle voor ons nodige gegevens en waarborgt U een stipte toezending van ons informatie-bulletin. Te laat gireren betekent indien de delen geheel uitverkocht zijn, dat U deze ontbreken want herdruk is niet mogelijk.

SINDS januari 1972 ontplooien wij onze activiteiten vanuit ons bedrijfspand aan de Spoorsingel 49 te Rotterdam-3004 (Blijdorp-zijde Centraal Station te Rotterdam) en hebben tevens een serie nieuwe kommunikatiemiddelen in gebruik genomen, waaronder

TELEFOON: 010 - 67 00 22 (4 lijnen)

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Via deze kommunikatiemiddelen zijn al onze afdelingen snel bereikbaar en kunnen wij onze service internationaal en opmimaal doen laten functioneren.

TOT ZIENS BIJ VAN DAM ELEKTRONICA AAN DE SPOORSINGEL 49 TE ROTTERDAM-3004

DIT IS DE NIEUWE WEG NAAR UW ELEKTRONICA LEVERANCIER

LAAT GERUST UW AUTO THUIS!

WIJ ZIJN NU EENVOUDIG TE BEREIKEN PER:

METRO

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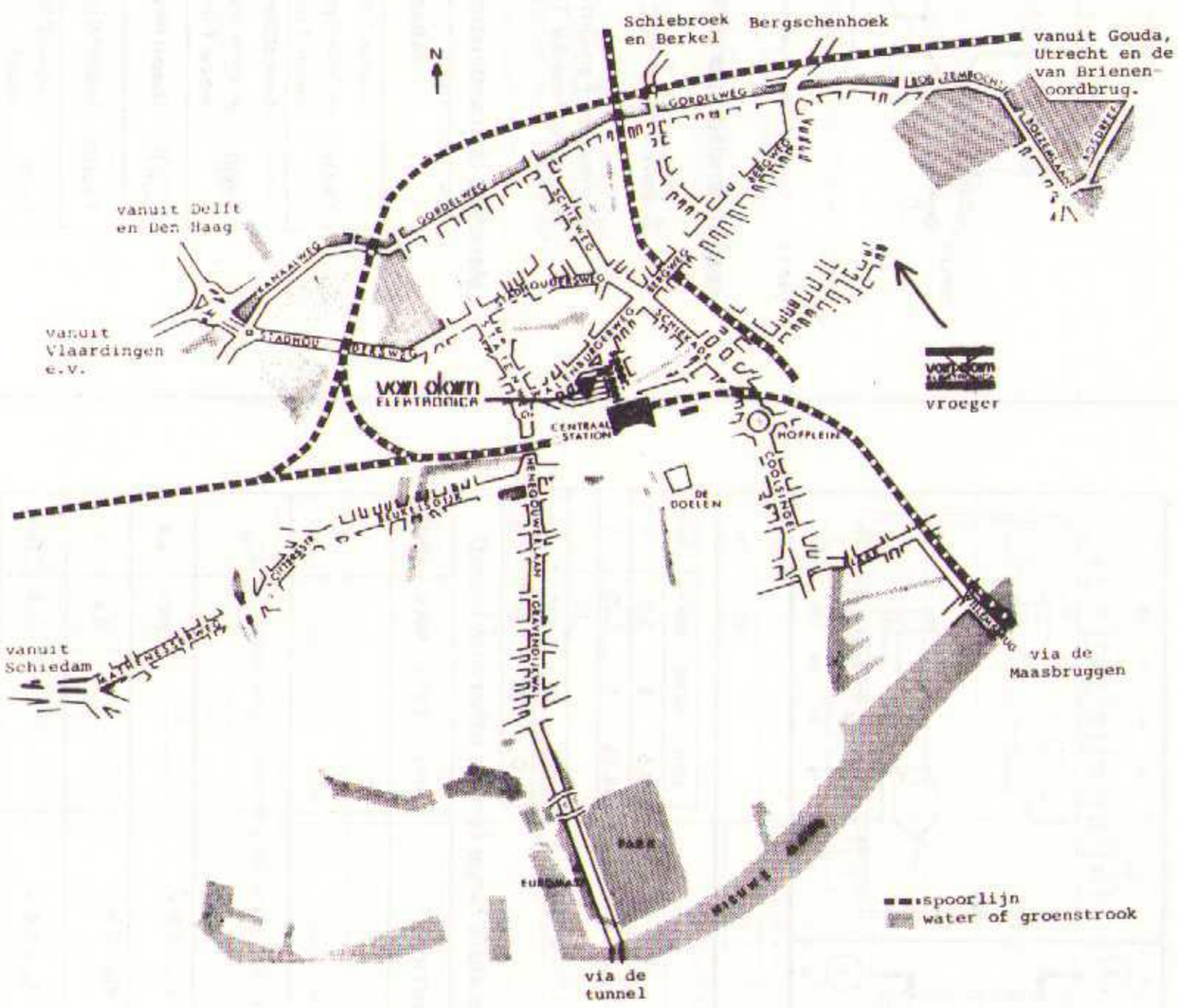

van dam
ELEKTRONICA

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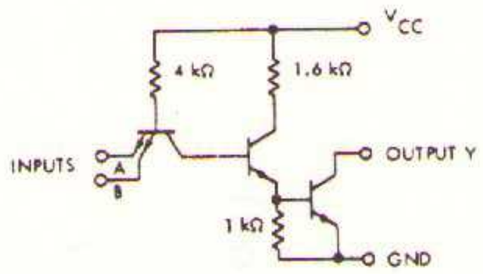
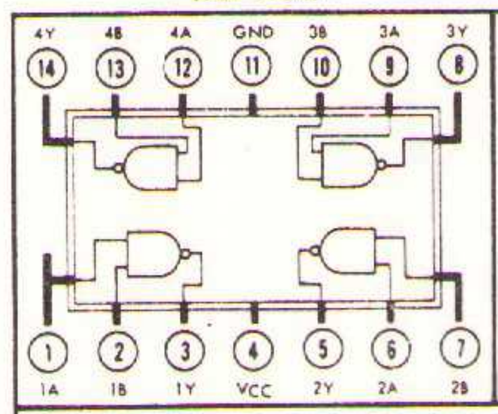
SN 7401 — quadruple 2-input positive nand gates (with open-collector output)

schematic (each gate)

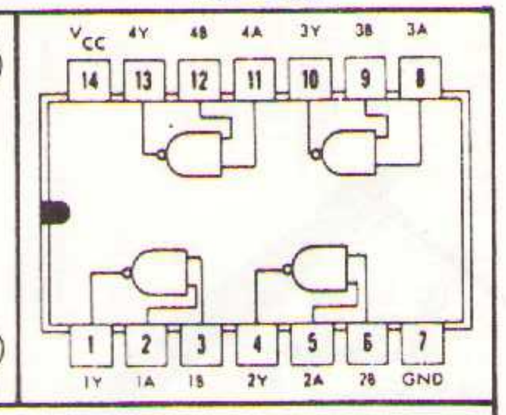


NOTE: Component values shown are nominal.

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5401 Circuits	4.5	5	5.5	V
	SN7401 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5401 Circuits	−55	25	125	°C
	SN7401 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

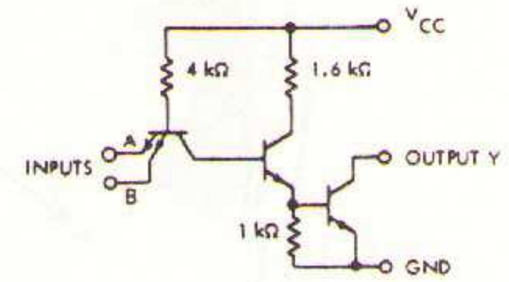
PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

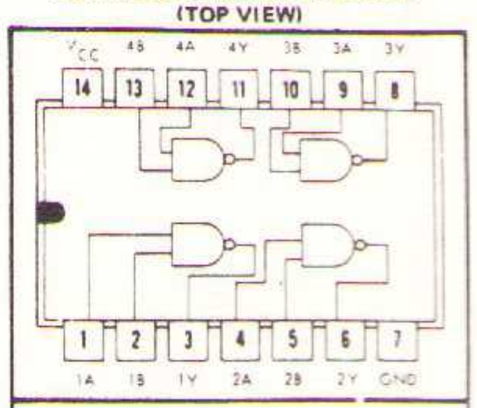
SN 7403 — quadruple 2-input positive nand gates (with open-collector output)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{AB}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5403 Circuits	4.5	5	5.5	V
	SN7403 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)				10	
Operating Free-Air Temperature Range, T_A:	SN5403 Circuits	−55	25	125	°C
	SN7403 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output)	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		12	22	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		4	8	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

SN 7405

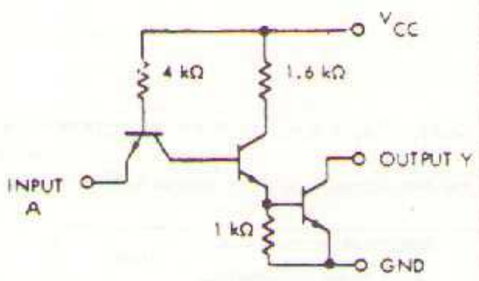
Hex inverters (with open-collector output)

SN 7406
SN 7416

hex inverter buffers/drivers with open-collector high-voltage outputs

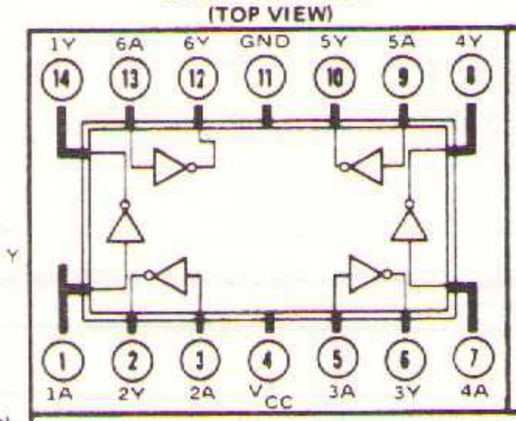
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS OR FOR DRIVING HIGH-CURRENT LOADS

chematic (each inverter)

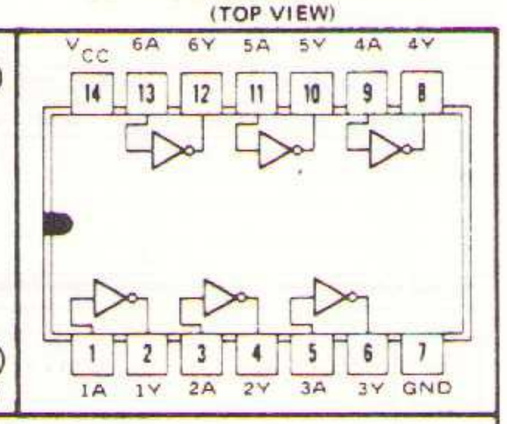


NOTE: Component values shown are nominal.

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic $Y = \overline{A}$

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: SN5405 Circuits	4.5	5	5.5	V
SN7405 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N (and see pages 2-7 and 2-8)			10	
Operating Free-Air Temperature Range, T_A: SN5405 Circuits	−55	25	125	°C
SN7405 Circuits	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

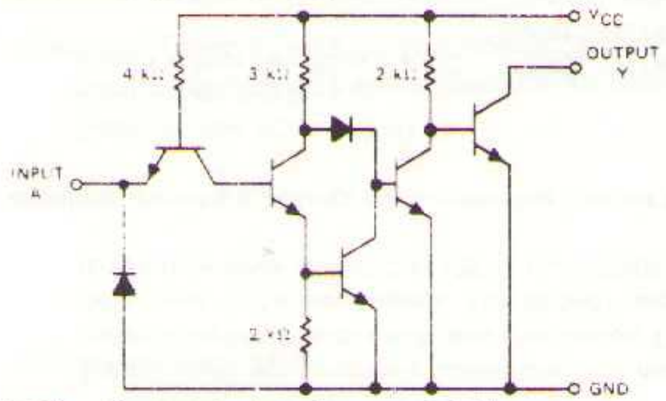
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at input terminal to ensure logical 0 (on) level at output	15			2			V
$V_{in(0)}$	Logical 0 input voltage required at input terminal to ensure logical 1 (off) level at output	17					0.8	V
$I_{out(1)}$	Output reverse current	17	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	V_{in} = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	15	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current	18	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current	18	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	20	V_{CC} = MAX, T_A = 25°C	V_{in} = 5 V,		18	33	mA
$I_{CC(1)}$	Logical 1 level supply current	20	V_{CC} = MAX, T_A = 25°C	V_{in} = 0,		6	12	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		40	55	ns

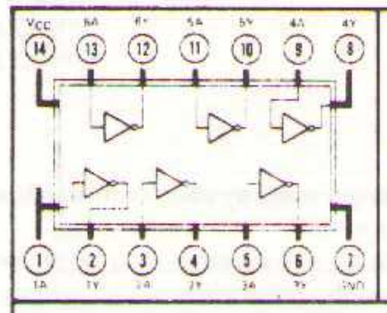
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ These typical values are at V_{CC} = 5 V, T_A = 25°C.

schematic (each inverter)

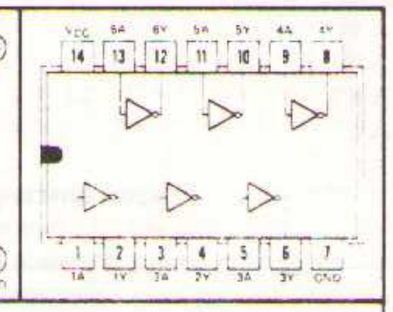


NOTE: Component values shown are nominal.

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{A}$

- Converts TTL voltage levels to MOS levels
- High sink-current capability
- Input clamping diodes simplify system design
- Typical propagation delay time: 15 ns
- Open-collector driver for indicator lamps and relays
- Inputs fully compatible with most TTL and DTL circuits
- Typical power dissipation: 105 mW

description

These monolithic TTL hex inverter buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as inverter buffers for driving TTL inputs. For increased fan-out, several inverters in a single package may be paralleled. The SN5406 and SN7406 have minimum breakdown voltages of 30 volts and the SN5416 and SN7416 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5406 and SN5416, and 40 milliamperes for the SN7406 and SN7416.

These circuits are completely compatible with most TTL or DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 150 milliwatts and average propagation delay time is 15 nanoseconds. The SN5406 and SN5416 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7406 and SN7416 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5406, SN7406 Circuits	30 V
	SN5416, SN7416 Circuits	15 V
Operating free-air temperature range:	SN5406, SN5416 Circuits	−55°C to 125°C
	SN7406, SN7416 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

SN 7407 SN 7417 — hex buffers/drivers with open collector high-voltage outputs

recommended operating conditions

		SN5406, SN5416			SN7406, SN7416			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5406, SN7406			30			30	V
	SN5416, SN7416			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	74		2			V
V_{IL}	Low-level input voltage	75				0.8	V
I_{OH}	High-level output current	75	V_{CC} = MIN, V_I = 0.8 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	74	V_{CC} = MIN, V_I = 2 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 2 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	76	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	77	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	78	V_{CC} = MAX, V_I = 0		30	42	mA
I_{CCL}	Supply current, low-level output	78	V_{CC} = MAX, V_I = 5 V		27	38	mA

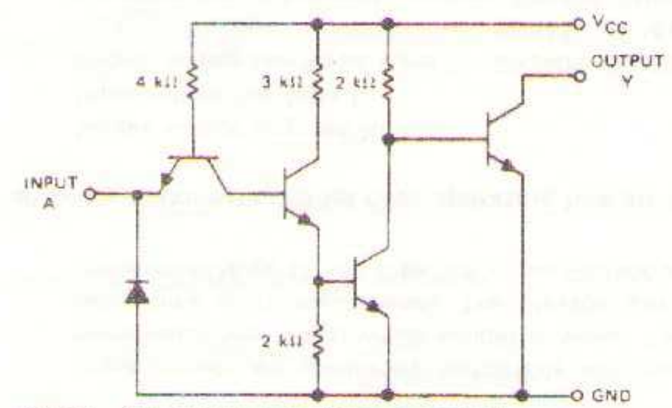
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	79	C_L = 15 pF, R_L = 110 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output	79	C_L = 15 pF, R_L = 110 Ω		15	23	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

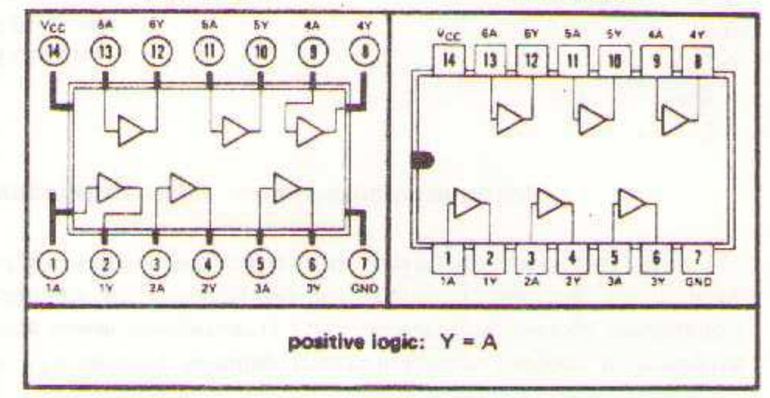
FOR INTERFACING WITH HIGH-LEVEL CIRCUITS OR FOR DRIVING HIGH-CURRENT LOADS

schematic (each buffer/driver)



NOTE: Component values shown are nominal.

W FLAT PACKAGE (TOP VIEW) — J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Y = A

- Converts TTL voltage levels to MOS levels
- High sink-current capability
- Input clamping diodes simplify system design
- Typical propagation delay time: 14 ns
- Open-collector driver for indicator lamps and relays
- Inputs fully compatible with most TTL and DTL circuits
- Typical power dissipation: 145 mW

description

These monolithic TTL hex buffers/drivers feature high-voltage open-collector outputs for interfacing with high-level circuits (such as MOS), or for driving high-current loads (such as lamps or relays), and are also characterized for use as buffers for driving TTL inputs. For increased fan-out, several buffers in a single package may be paralleled. The SN5407 and SN7407 have minimum breakdown voltages of 30 volts and the SN5417 and SN7417 have minimum breakdown voltages of 15 volts. The maximum sink current is 30 milliamperes for the SN5407 and SN5417, and 40 milliamperes for the SN7407 and SN7417.

These circuits are completely compatible with most TTL and DTL families. Inputs are diode-clamped to minimize transmission-line effects which simplifies design. Typical power dissipation is 145 milliwatts and average propagation delay time is 14 nanoseconds. The SN5407 and SN5417 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7407 and SN7417 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2):	SN5407, SN7407 Circuits	30 V
	SN5417, SN7417 Circuits	15 V
Operating free-air temperature range:	SN5407, SN5417 Circuits	−55°C to 125°C
	SN7407, SN7417 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN5407, SN5417			SN7407, SN7417			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}	SN5407, SN7407			30			30	V
	SN5417, SN7417			15			15	
Low-level output current, I_{OL}				30			40	mA
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	80		2			V
V_{IL}	Low-level input voltage	81				0.8	V
I_{OH}	High-level output current	80	V_{CC} = MIN, V_I = 2 V, V_{OH} = MAX			250	μA
V_{OL}	Low-level output voltage	81	V_{CC} = MIN, V_I = 0.8 V, I_{OL} = MAX			0.7	V
			V_{CC} = MIN, V_I = 0.8 V, I_{OL} = 16 mA			0.4	
I_{IH}	High-level input current (each input)	82	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	83	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	84	V_{CC} = MAX, V_I = 5 V		29	41	mA
I_{CCL}	Supply current, low-level output	84	V_{CC} = MAX, V_I = 0		21	30	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

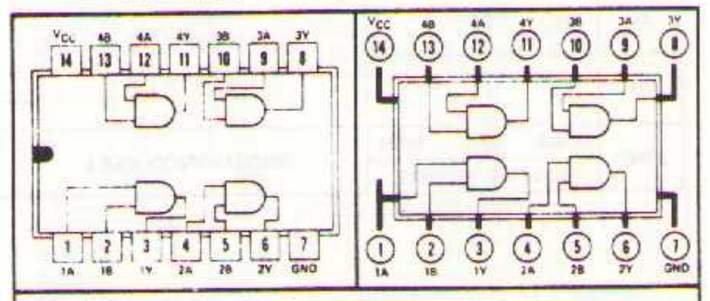
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	85	C_L = 15 pF, R_L = 110 Ω		6	10	ns
t_{PHL}	Propagation delay time, high-to-low-level output	85	C_L = 15 pF, R_L = 110 Ω		20	30	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

Choice of Totem-Pole Outputs (SN5408/SN7408) or Open-Collector Outputs (SN5409/SN7409)

J OR N
DUAL-IN-LINE PACKAGE
(TOP VIEW)

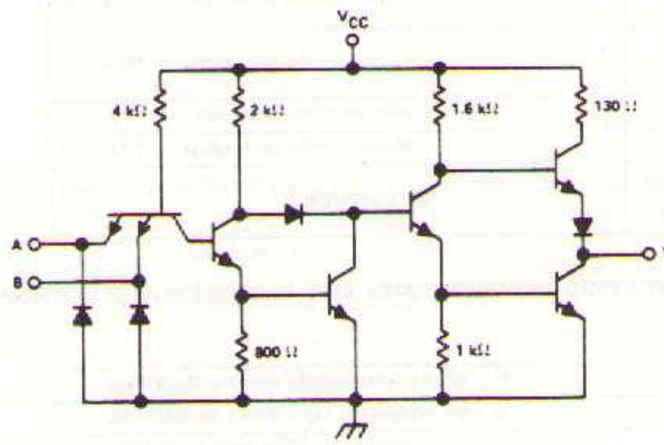
W
FLAT PACKAGE
(TOP VIEW)



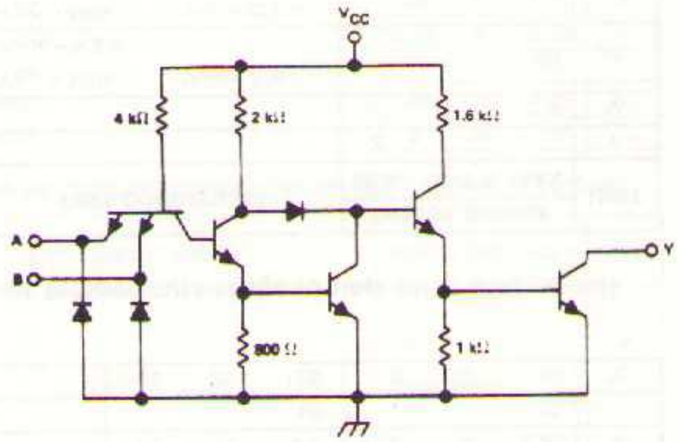
positive logic: Y = AB

schematics (each gate)

SN5408, SN7408



SN5409, SN7409



Component values shown are nominal.

description

These Series 54/74 TTL gates provide the system designer with direct implementation of the positive AND or negative OR functions.

The SN5408/SN7408, with totem-pole outputs, drives 10 normalized Series 54/74 loads at the low output level and 20 loads at the high output level. The SN5409/SN7409, with open-collector output, provides additional logic flexibility, as the outputs may be wire-AND connected to extend the AND function. The SN5409/SN7409 will sink sufficient current to drive 10 normalized Series 54/74 loads at the low output level.

The SN5408 and SN5409 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN7408 and SN7409 are characterized for operation from 0°C to 70°C.

SN5408, SN7408

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range, T_A:	SN5408 Circuits	−55°C to 125°C
	SN7408 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

	SN5408			SN7408			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN5408, SN7408 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	86			2			V
V_{IL}	Low-level input voltage	88					0.8	V
V_{OH}	High-level output voltage	86	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	91	V_{CC} = MAX	SN5408	−20		−55	mA
				SN7408	−18		−55	
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX,	V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX,	V_I = 0		20	33	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5408, SN7408 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF, R_L = 400 Ω		17.5	27	ns
t_{PHL}	Propagation delay time, high-to-low-level output				12	19	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output shbuld be shorted at a time.

SN5409, SN7409

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Output voltage (see Notes 1 and 3)		5.5 V
Operating free-air temperature range:	SN5409 Circuits	−55°C to 125°C
	SN7409 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5409			SN7409			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN5409, SN7409 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	87			2			V
V_{IL}	Low-level input voltage	88					0.8	V
I_{OH}	High-level output current	87	V_{CC} = MIN, V_{OH} = 5.5 V	V_{IH} = 2 V,			250	μA
V_{OL}	Low-level output voltage	88	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_{IH}	High-level input current (each input)	89	V_{CC} = MAX,	V_I = 2.4 V			40	μA
			V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	90	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	92	V_{CC} = MAX,	V_I = 5 V		11	21	mA
I_{CCL}	Supply current, low-level output	92	V_{CC} = MAX,	V_I = 0		20	33	mA

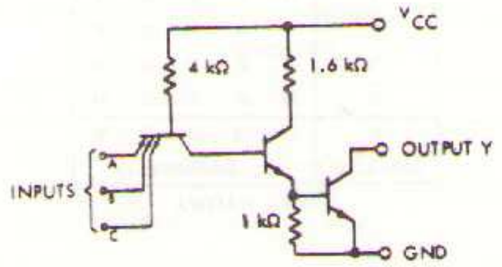
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	SN5409, SN7409 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	93	C_L = 15 pF R_L = 400 Ω		21	32	ns
t_{PHL}	Propagation delay time, high-to-low-level output				16	24	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

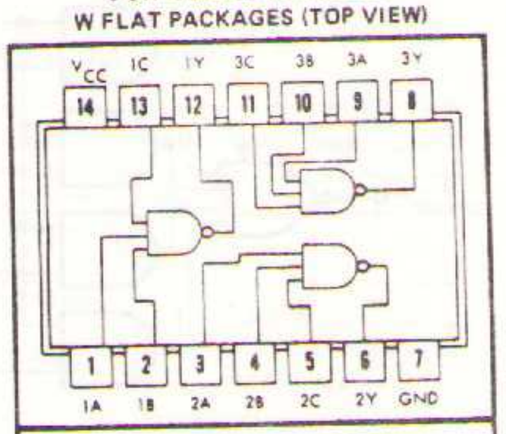
SN 7412 — triple 3-input positive nand gates (with open-collector output)

schematic (each gate)



NOTE: Component values shown are nominal.

J OR N DUAL-IN-LINE OR W FLAT PACKAGES (TOP VIEW)



positive logic: $Y = \overline{ABC}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5412 Circuits	4.5	5	5.5	V
	SN7412 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5412 Circuits	−55	25	125	°C
	SN7412 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at both input terminals to ensure logical 0 (on) level at output	1			2			V
$V_{in(0)}$	Logical 0 input voltage required at either input terminal to ensure logical 1 (off) level at output	7					0.8	V
$I_{out(1)}$	Output reverse current	7	V_{CC} = MIN, $V_{out(1)}$ = 5.5 V	$V_{in(0)}$ = 0.8 V,			250	μA
$V_{out(0)}$	Logical 0 output voltage (on level)	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V		9	16.5	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0		3	6	mA

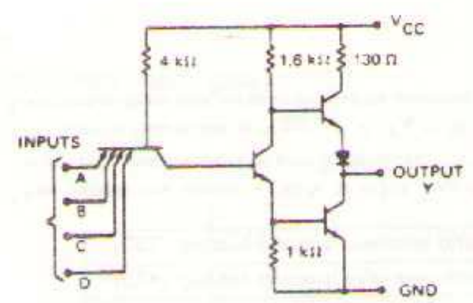
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 4 kΩ		35	45	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating condionts for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

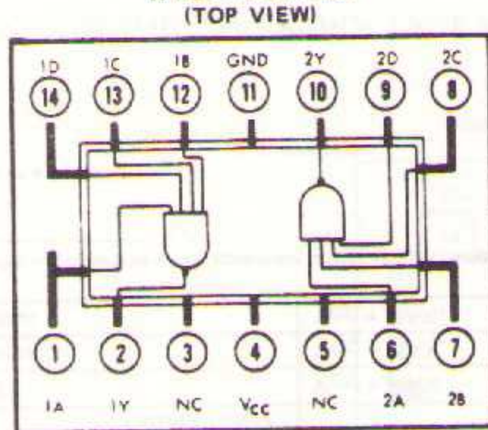
SN 7420 — dual 4-input positive nand gates

schematic (each gate)

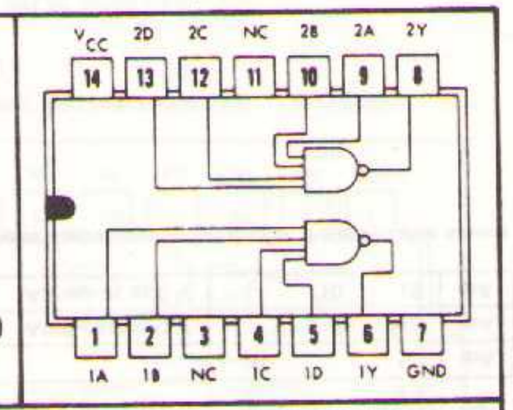


Component values shown are nominal.
NC—No Internal Connection

W FLAT PACKAGE (TOP VIEW)



J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: $Y = \overline{ABCD}$

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}:	SN5420 Circuits	4.5	5	5.5	V
	SN7420 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output, N				10	
Operating Free-Air Temperature Range, T_A:	SN5420 Circuits	−55	25	125	°C
	SN7420 Circuits	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

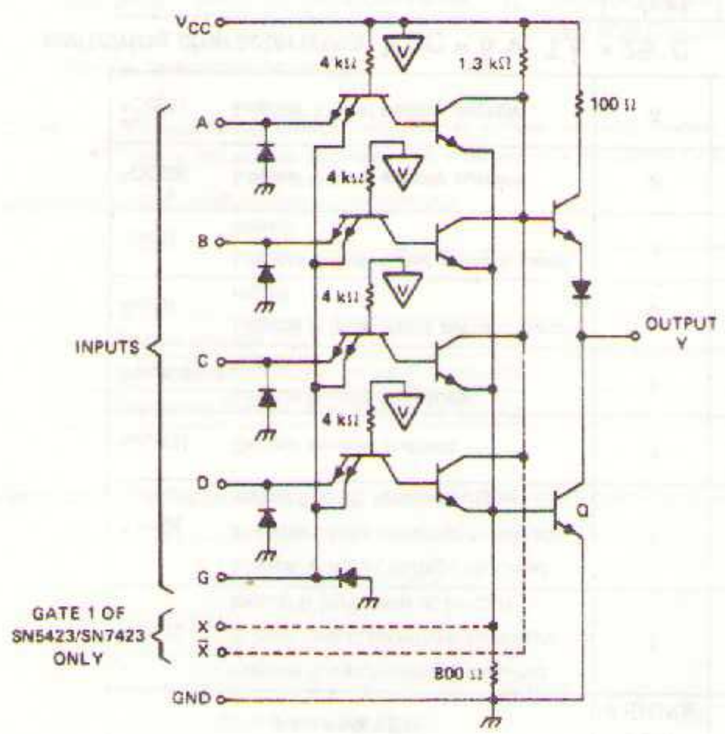
PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage required at all input terminals to ensure logical 0 level at output	1				2			V
$V_{in(0)}$	Logical 0 input voltage required at any input terminal to ensure logical 1 level at output	2						0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, I_{load} = −400 μA	V_{in} = 0.8 V,		2.4	3.3		V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, I_{sink} = 16 mA	V_{in} = 2 V,			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX		SN5420	−20		−55	mA
					SN7420	−18		−55	
$I_{CC(0)}$	Logical 0 level supply current	6	V_{CC} = MAX,	V_{in} = 5 V			6	11	mA
$I_{CC(1)}$	Logical 1 level supply current	6	V_{CC} = MAX,	V_{in} = 0			2	4	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level	65	C_L = 15 pF,	R_L = 400 Ω		8	15	ns
t_{pd1}	Propagation delay time to logical 1 level	65	C_L = 15 pF,	R_L = 400 Ω		12	22	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

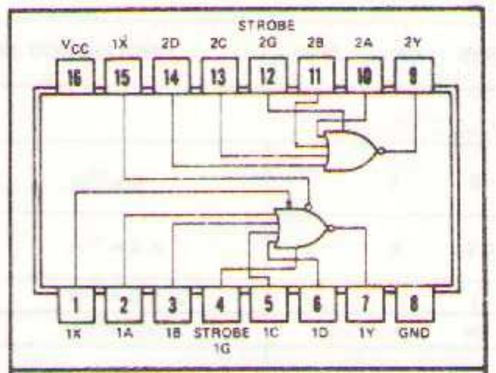
schematic (each gate)



NOTES: A. Component values shown are nominal.
B. Both expander inputs are used simultaneously for expanding.
C. If expander is not used leave X and X̄ open.
D. A total of four expander gates can be connected to the expander inputs.

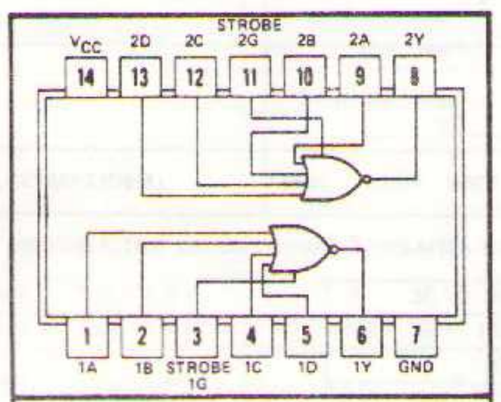
▽ – V_{CC} bus

SN5423, SN7423
J OR N DUAL-IN-LINE OR W FLAT PACKAGES (TOP VIEW)†



positive logic:
$1Y = \overline{1G(1A+1B+1C+1D)+X}$
$2Y = \overline{2G(2A+2B+2C+2D)}$
X = output of SN5460/SN7460

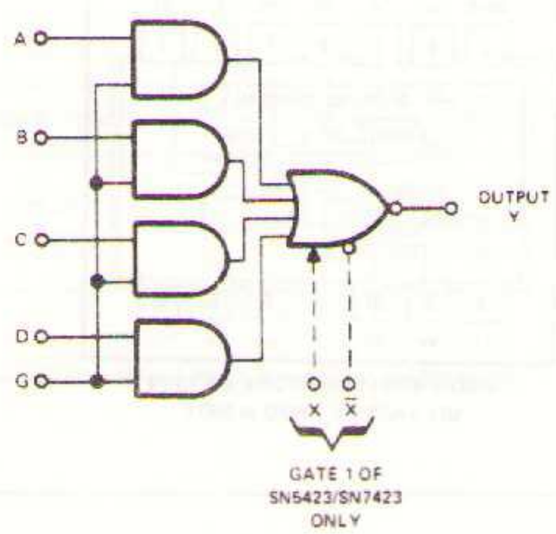
SN5425, SN7425
J OR N DUAL-IN-LINE OR W FLAT PACKAGES (TOP VIEW)†



positive logic:
$Y = \overline{G(A+B+C+D)}$

†Pin assignments for these circuits are the same for all packages.

logic and functional block diagram (each gate)



TRUTH TABLE

INPUTS					OUTPUT
A	B	C	D	G	Y
H	X	X	X	H	L
X	H	X	X	H	L
X	X	H	X	H	L
X	X	X	H	H	L
L	L	L	L	X	H
X	X	X	X	L	H

Expander inputs are open.
H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5423, SN5425 Circuits	−55°C to 125°C
SN7423, SN7425 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor.

recommended operating conditions

		SN5423, SN5425			SN7423, SN7425			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA	V_{IL} = 0.8 V,	2.4	3.3		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		strobe inputs					160	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		strobe inputs					−6.4	
I_{OS}	Short-circuit output current§		V_{CC} = MAX		−20		−55	mA
I_{CCH}	Supply current, high-level output		V_{CC} = MAX,	All inputs at 0 V		8	16	mA
I_{CCL}	Supply current, low-level output		V_{CC} = MAX,	All inputs at 5 V		10	19	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type. Expander inputs X and X̄ are open.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

electrical characteristics (SN5423 circuits) using expander inputs, V_{CC} = 4.5 V, T_A = −55°C

PARAMETER		TEST FIGURE¶	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{OL} = 16 mA			2.9	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{OL} = 16 mA, I_1 = 0.41 mA, R_1 = 0			1	V
V_{OH}	High-level output voltage	30	I_{OH} = −400 μA, I_1 = 0.15 mA, I_2 = −0.15 mA	2.4	3.3		V
V_{OL}	Low-level output voltage	29	I_{OL} = 16 mA, I_1 = 0.3 mA, R_1 = 138 Ω		0.22	0.4	V

electrical characteristics (SN7423 circuits) using expander inputs, V_{CC} = 4.75 V, T_A = 0°C

PARAMETER		TEST FIGURE¶	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
I_X	Expander current	28	V_1 = 0.4 V, I_{OL} = 16 mA			3.1	mA
$V_{BE(Q)}$	Base-emitter voltage of output transistor (Q)	29	I_{OL} = 16 mA, I_1 = 0.62 mA, R_1 = 0			1	V
V_{OH}	High-level output voltage	30	I_{OH} = −400 μA, I_1 = 270 μA, I_2 = −270 μA	2.4	3.3		V
V_{OL}	Low-level output voltage	29	I_{OL} = 16 mA, I_1 = 0.43 mA, R_1 = 130 Ω		0.22	0.4	V

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Referenced test figures appear on page 2-49 of TTL Integrated Circuits Catalog (CC201).

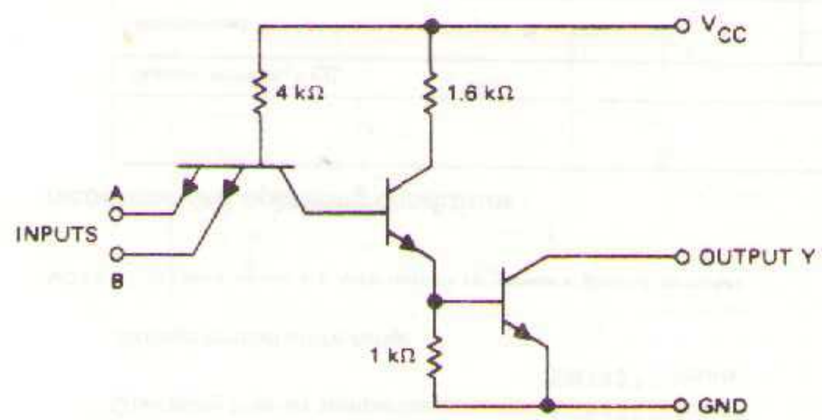
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, (see note 3)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 15 pF, R_L = 400 Ω		13	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		8	15	ns

NOTE 3: Switching characteristics of the SN5423 and SN7424 are tested with the expander pins open.

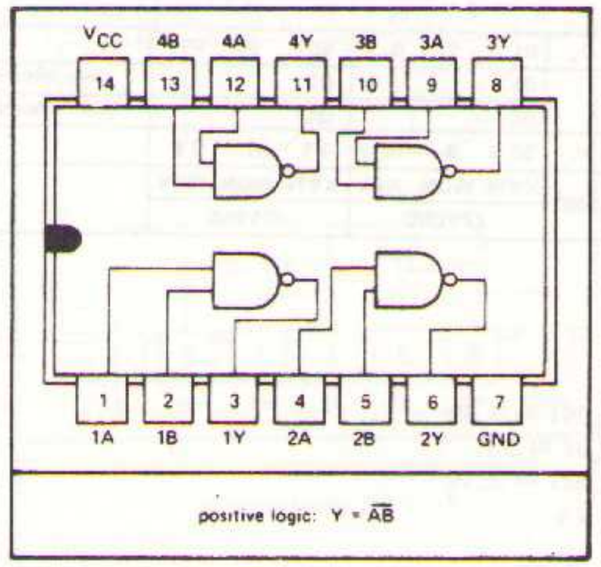
FOR DRIVING LOW-THRESHOLD-VOLTAGE MOS INPUTS

schematic (each gate)



Component values shown are nominal.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

These open-collector NAND gates feature high output voltage ratings for interfacing with low-threshold-voltage MOS logic circuits or other 12-volt systems. Although the output is rated to withstand 15 volts, the V_{CC} terminal is connected to the standard 5-volt source. The output transistor will sink 16 milliamperes while maintaining a low-level output voltage of 0.4 volt maximum thus providing a high-fan-out driver with the nominal power dissipation of standard Series 54/74 gates.

The SN5426 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7426 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Output voltage (see Notes 1 and 2) . . . . . 15 V
Operating free-air temperature range: SN5426 Circuits . . . . . −55°C to 125°C
SN7426 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5426			SN7426			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage	4.5	5	5.5	4.75	5	5.25	V
Output voltage, V_{OH}			15			15	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

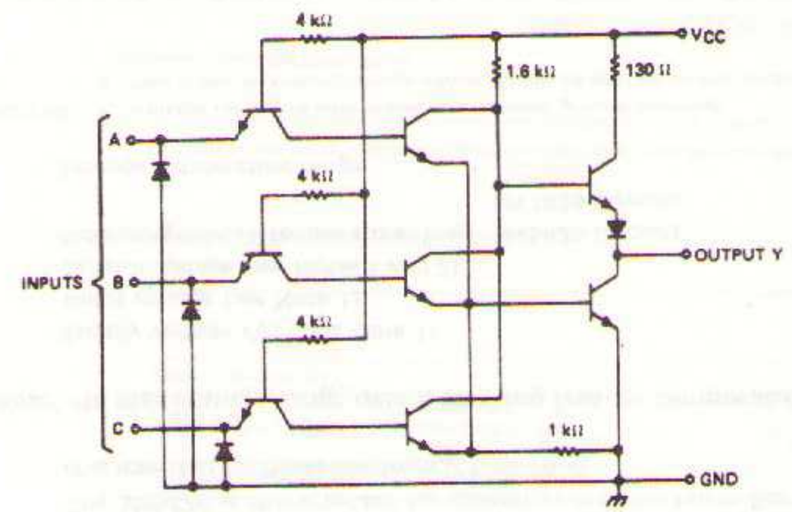
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	101		2			V
V_{IL}	Low-level input voltage	102				0.8	V
V_{OH}	High-level output voltage	102	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OH} = 1 mA	15			V
I_{OH}	High-level output current	102	V_{CC} = MIN, V_{IL} = 0.8 V, V_{OH} = 12 V			50	μA
V_{OL}	Low-level output voltage	101	V_{CC} = MIN, V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (each input)	103	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (each input)	104	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{CCH}	Supply current, high-level output	105	V_{CC} = MAX, V_I = 0		4	8	mA
I_{CCL}	Supply current, low-level output	105	V_{CC} = MAX, V_I = 5 V		12	22	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

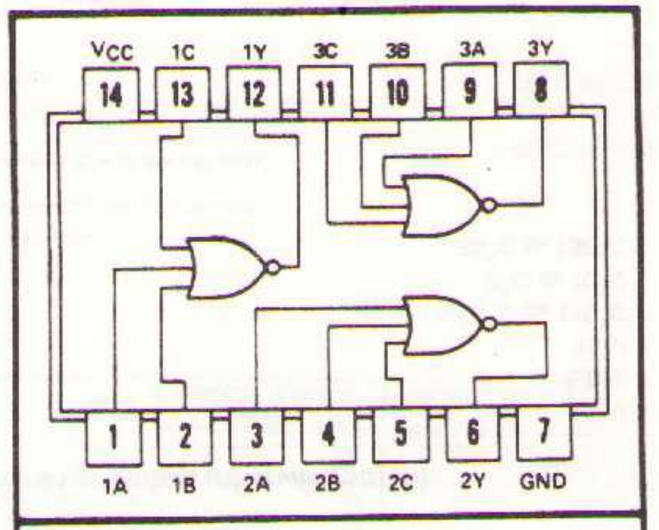
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	106	C_L = 15 pF, R_L = 1 kΩ		16	24	ns
t_{PHL}	Propagation delay time, high-to-low-level output	106	C_L = 15 pF, R_L = 1 kΩ		11	17	ns

schematic (each gate)



Component values shown are nominal.

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: $Y = \overline{A + B + C}$

†Pin assignments for these circuits are the same for all packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5427 Circuits . . . . . −55°C to 125°C
SN7427 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5427			SN7427			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

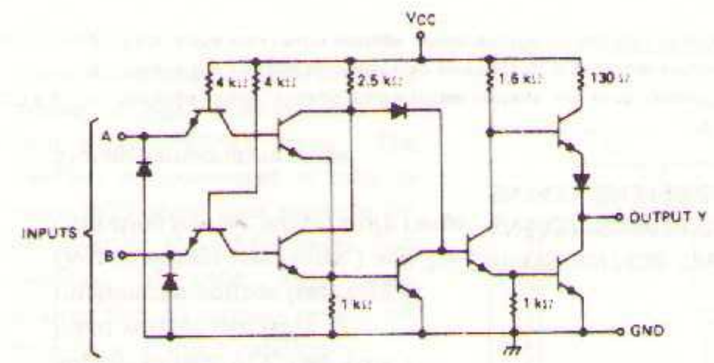
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA	V_{IL} = 0.8 V,	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IH} = 2 V,		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN5427	−20		−55	mA
			SN7427	−18		−55	
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		10	16	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		16	26	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTES: 2. I_{CCH} is measured with all inputs grounded, and outputs open.
3. I_{CCL} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.

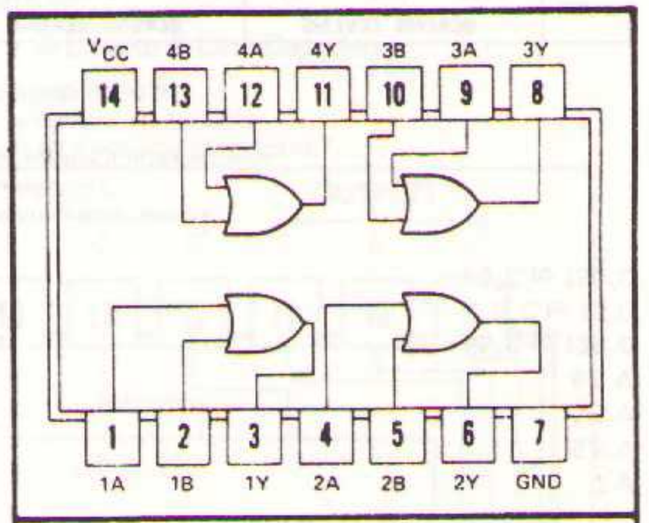
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		10	15	ns
t_{PLH}	Propagation delay time, low-to-high-level output			7	11	ns

schematic (each gate)



J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: Y = A + B

†Pin assignments for these circuits are the same for all packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage . . . . . 5.5 V
Operating free-air temperature range: SN5432 Circuits . . . . . −55°C to 125°C
SN7432 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE: 1. Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN5432			SN7432			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4	3.3		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN5432	−20		−55	mA
			SN7432	−18		−55	
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	See Note 2		15	22	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	See Note 3		23	38	mA

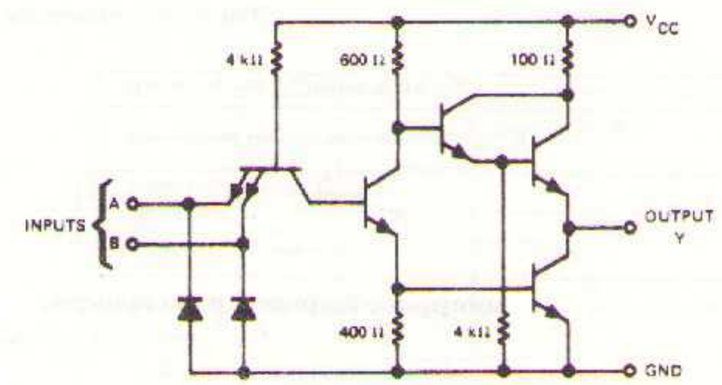
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTES: 2. I_{CCH} is measured with one input of each gate at 4.5 V, the remaining inputs grounded, and outputs open.
3. I_{CCL} is measured with both inputs of all gates grounded, and outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

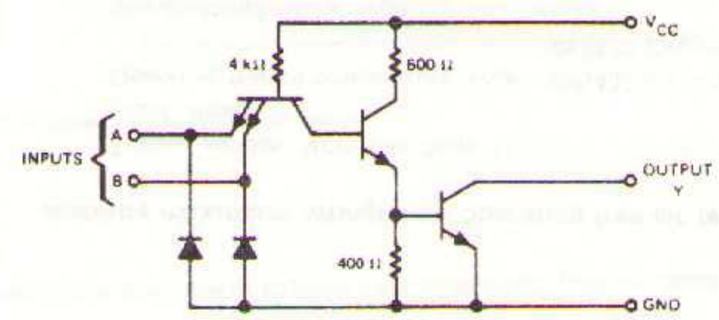
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high-to-low-level output	C_L = 15 pF, R_L = 400 Ω		14	22	ns
t_{PLH}	Propagation delay time, low-to-high-level output			10	15	ns

schematics (each buffer)

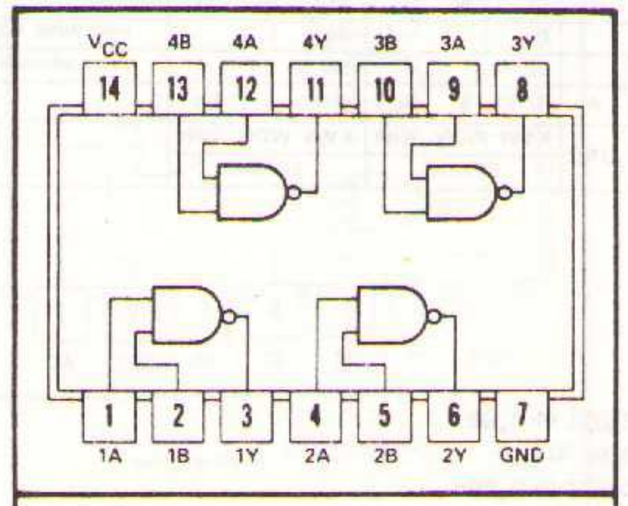
SN5437, SN7437 (TOTEM-POLE OUTPUT)



SN5438, SN7438 (OPEN-COLLECTOR OUTPUT)



J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: $Y = \overline{AB}$

† Pin assignments for these circuits are the same for all packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Output voltage (see Notes 1 and 3): SN5438, SN7438 Circuits . . . . . 5.5 V
Operating free-air temperature range: SN5437, SN5438 Circuits . . . . . −55°C to 125°C
SN7437, SN7438 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor.
3. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

	SN5437, SN5438			SN7437, SN7438			UNIT
	MIN	TYP	MAX	MIN	TYP	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			30			30	
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN5437, SN7437 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, I_{OH} = −1.2 mA	V_{IL} = 0.8 V,	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 48 mA	V_{IH} = 2 V,		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX,	V_I = 0	−20		−70	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	All inputs at 0 V		9	15.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	All inputs at 5 V		34	54	mA

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			SN5438, SN7438 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA				−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_{IL} = 0.8 V,	V_{OH} = 5.5 V			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN,	V_{IH} = 2 V,	I_{OL} = 48 mA		0.22	0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
I_{CCH}	Supply current, high-level output	V_{CC} = MAX,	All inputs at 0 V			5	8.5	mA
I_{CCL}	Supply current, low-level output	V_{CC} = MAX,	All inputs at 5 V			34	54	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short-circuit test should not exceed one second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 30

PARAMETER		TEST CONDITIONS	SN5437, SN7437 MIN	TYP	MAX	SN5438, SN7438 MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 45 pF, R_L = 133 Ω		13	22		14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output			8	15		11	18	ns

- BCD-to-Decimal
- Excess-3-to-Decimal
- Excess-3-Gray-to-Decimal

Also for applications as

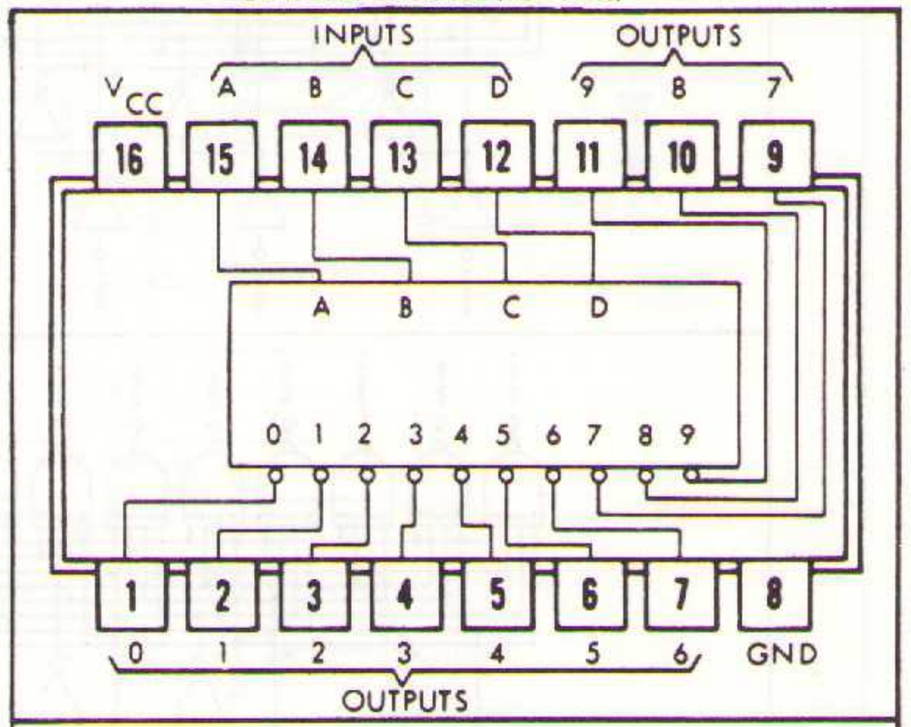
- 4-Line-to-16-Line Decoders
- 3-Line to 8-Line Decoders
- featuring diode-clamped inputs

description

These monolithic decimal decoders consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid input logic ensures that all outputs remain off for all invalid input conditions.

The SN5442/SN7442 BCD-to-decimal, SN5443/SN7443 excess-3-to-decimal, and SN5444/SN7444 excess-3-gray-to-decimal decoders feature familiar transistor-transistor-logic (TTL) circuits with inputs and outputs which are compatible for use with other TTL and DTL circuits. D-c noise margins are typically one volt and power dissipation is typically 140 milliwatts. Full fan-out of 10 is available at all outputs.

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth tables

†Pin assignments for these circuits are the same for all packages.

SN5442/SN7442 BCD INPUT				SN5443/SN7443 EXCESS 3 INPUT				SN5444/SN7444 EXCESS 3 GRAY INPUT				ALL TYPES DECIMAL OUTPUT									
D	C	B	A	D	C	B	A	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	1	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	0	1	0	0	0	1	1	0	1	0	1	1	1	1	1	1	1	1
0	0	1	0	0	1	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1
0	0	1	1	0	1	1	0	0	1	0	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	0	1	1	1	0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	0	0	0	1	1	0	0	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	0	0	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	0	1	1	1	1	1	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	0	0	1	0	1	0	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage, V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN5442, SN5443, SN5444 Circuits	−55°C to 125°C
	SN7442, SN7443, SN7444 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5442, SN5443, SN5444 Circuits	4.5	5	5.5	V
SN7442, SN7443, SN7444 Circuits	4.75	5	5.25	V
Normalized Fan-Out from each Output (N)			10	

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN5442, SN5443, SN5444	−20		−55	mA
				SN7442, SN7443, SN7444	−18		−55	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5442, SN5443, SN5444		28	41	mA
				SN7442, SN7443, SN7444		28	56	mA

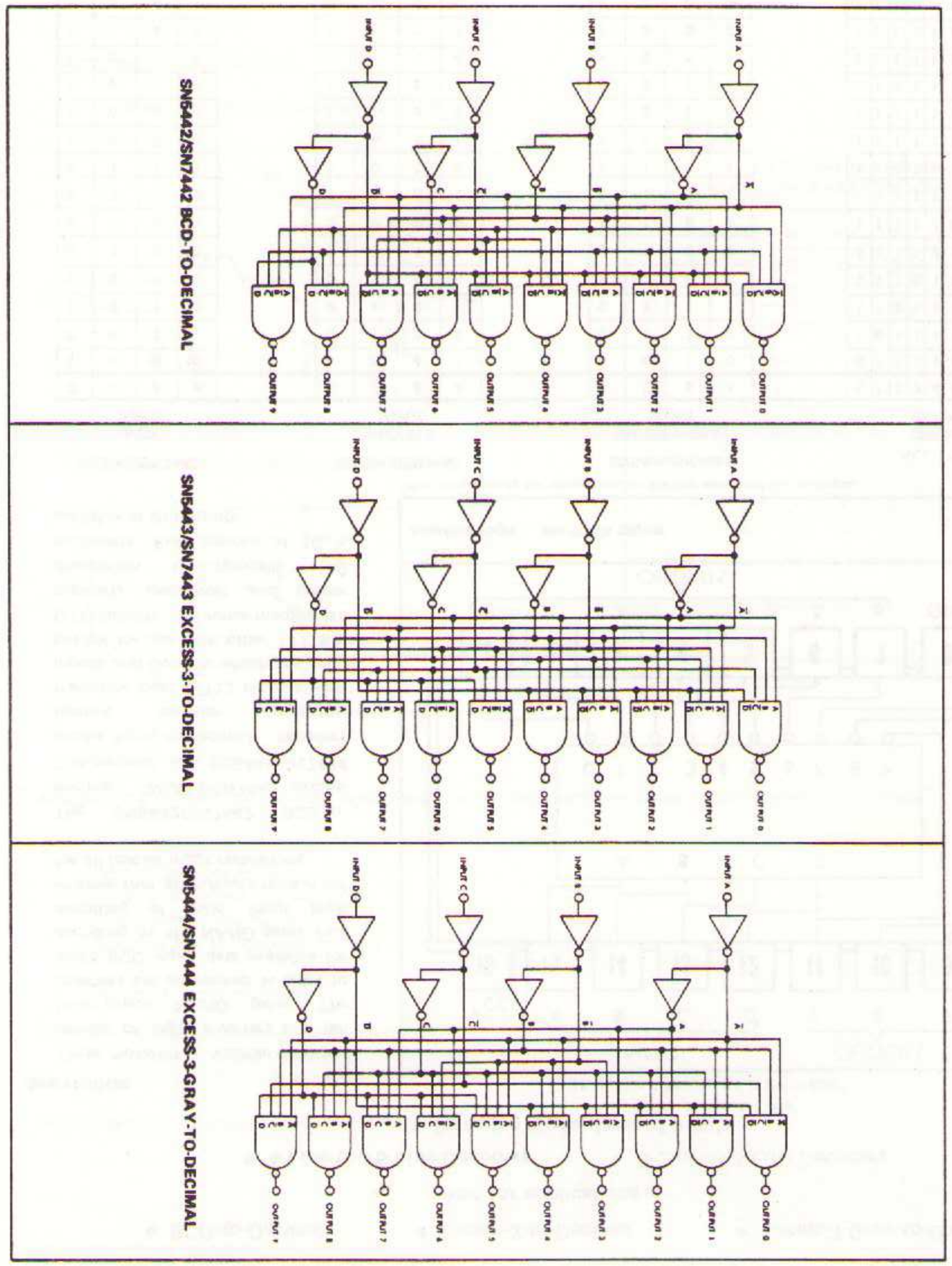
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	Propagation delay time to logical 0 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	22	30	ns
t_{pd0}	Propagation delay time to logical 0 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		23	35	ns
t_{pd1}	Propagation delay time to logical 1 level through two logic levels	6	C_L = 15 pF, R_L = 400 Ω	10	17	25	ns
t_{pd1}	Propagation delay time to logical 1 level through three logic levels	6	C_L = 15 pF, R_L = 400 Ω		26	35	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

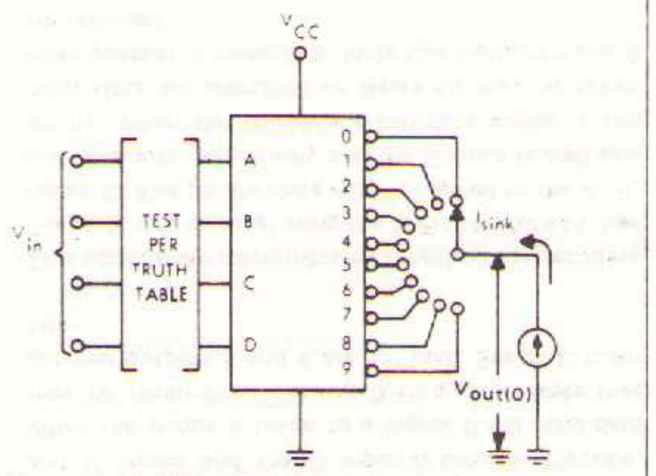
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.



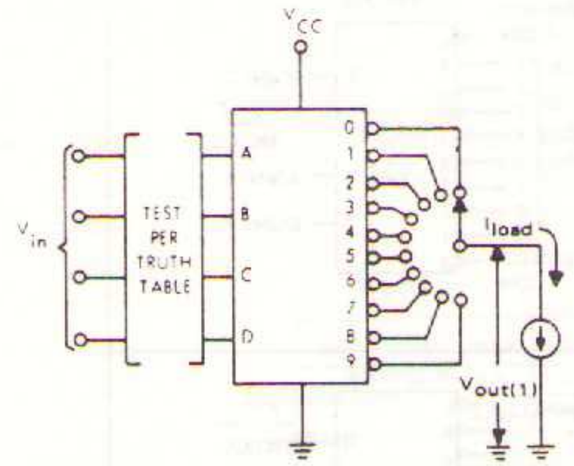
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



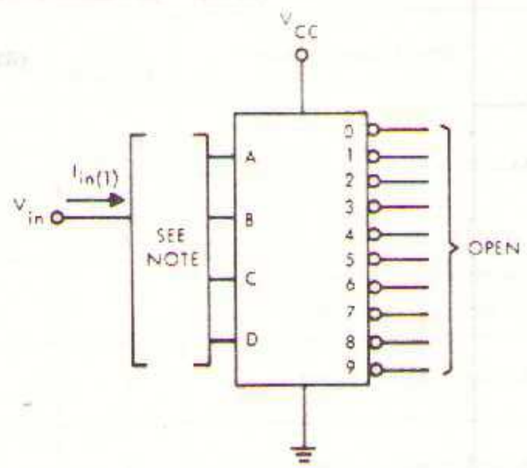
1. Each output is tested separately.

FIGURE 1



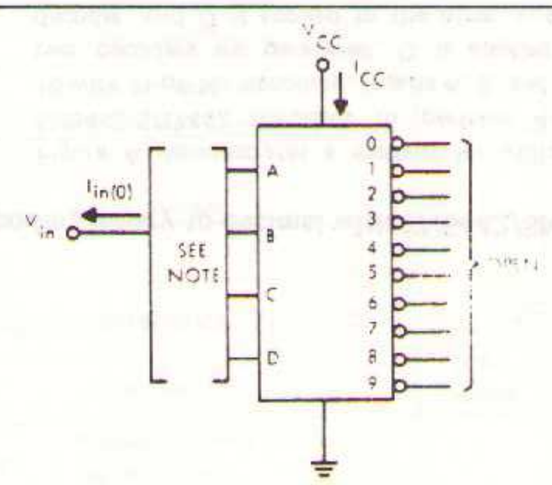
1. Each output is tested separately.

FIGURE 2



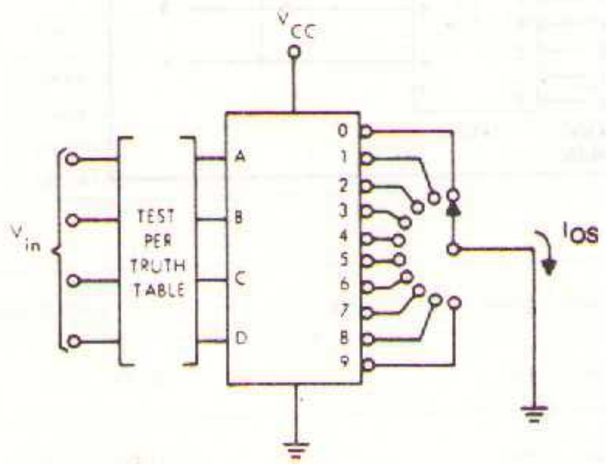
1. Each input is tested separately.

FIGURE 3



1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4

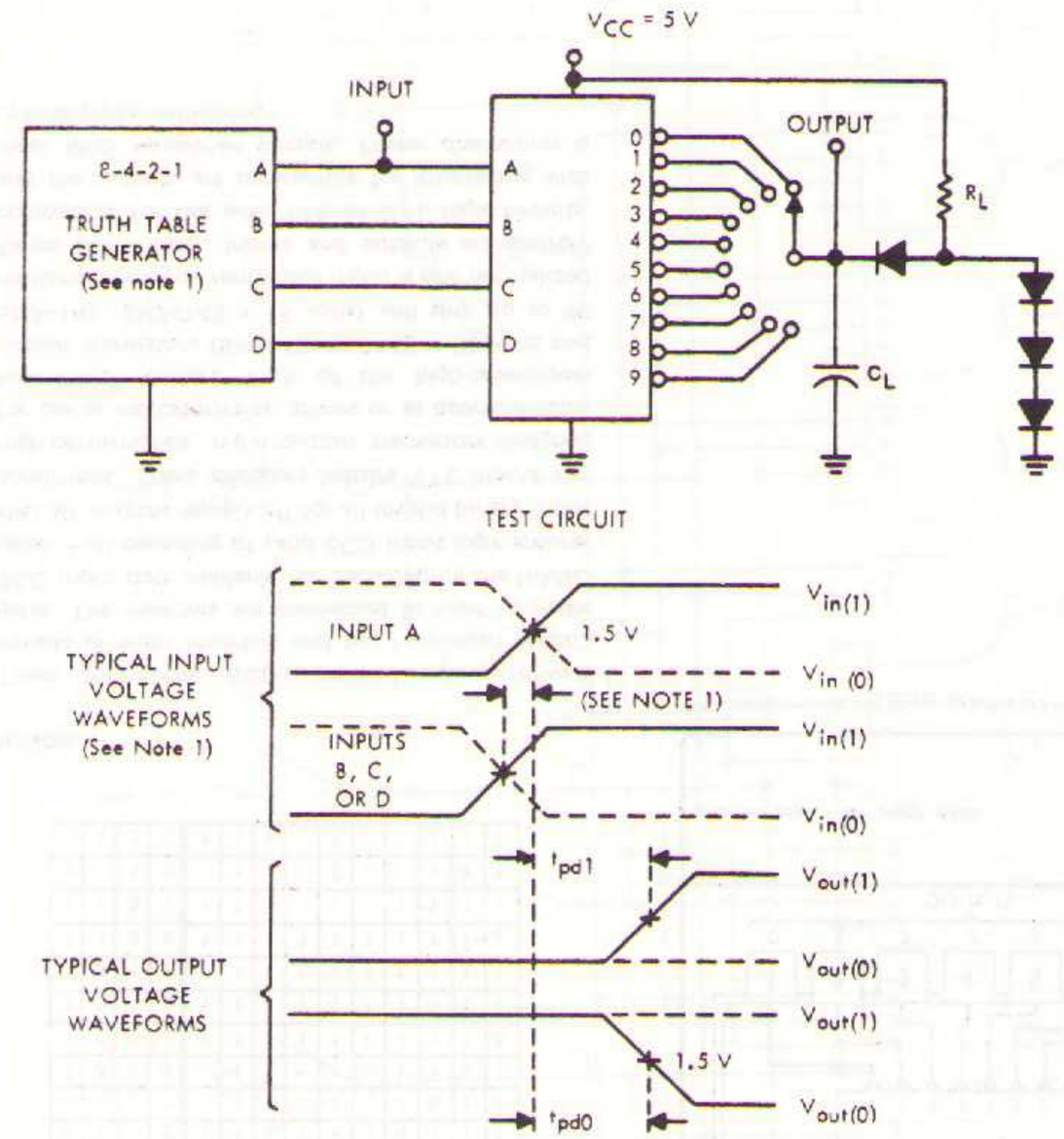


1. Each output is tested separately.

FIGURE 5

†Arrows indicate actual direction of current flow

switching characteristics



NOTES: 1. The truth table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Input B, C, and D transitions occur simultaneously with or prior to input A transistions.

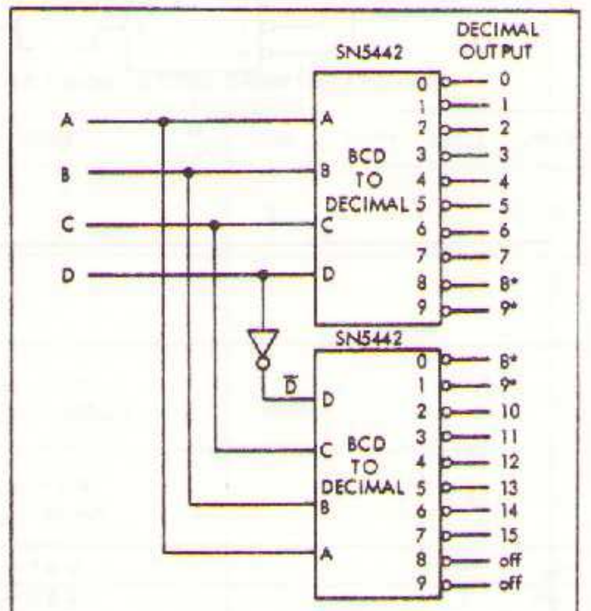
2. C_L includes probe and jig capacitance.
3. All diodes are 1N3064.

FIGURE 6—SWITCHING TIMES

TYPICAL APPLICATIONS

decoding binary-to-decimal with SN5442/SN7442,

Figure A demonstrates a method for utilizing two SN5442/SN7442 decoders to perform 4-wire to 16-wire (1-of-16) decoding. Inputs A, B, and C of the two decoders are paralleled, D is applied to one decoder, and $\overline{D}$ is applied to the other as shown in figure A. Decimal equivalents are available as indicated. Note that decimal 8 and 9 are available from both decoders.



*These decimal outputs are available from both decoders.

FIGURE A

decoding 3-wire binary-to-octal

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5442/SN7442. See figure B. The binary code ABC is applied to the A, B, and C inputs and the D input is used as a strobe. When the strobe is taken to a logical 0 the octal data may be taken from outputs 0 through 7. Note that decimal outputs 8 and 9 are not used. See BCD truth table.

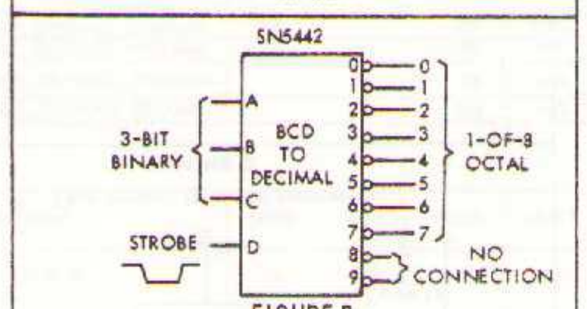


FIGURE B

This application demonstrates a method for decoding 3-wire binary-to-octal using the SN5444/SN7444. See figure C. The binary code ABC is applied to the A, B, and D inputs respectively and the C input is used as a strobe. When the strobe is taken to a logical 1 the octal data (as identified in figure C) may be taken from outputs 1 through 8. Note that outputs 0 and 9 are not used.

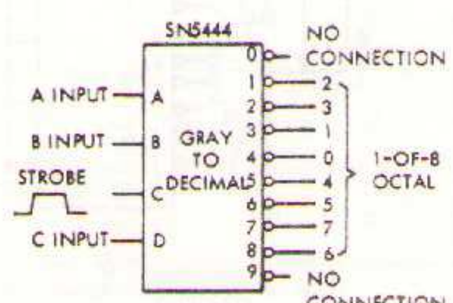


FIGURE C

TTL MSI LAMP, LOGIC, OR MOS DRIVERS

featuring

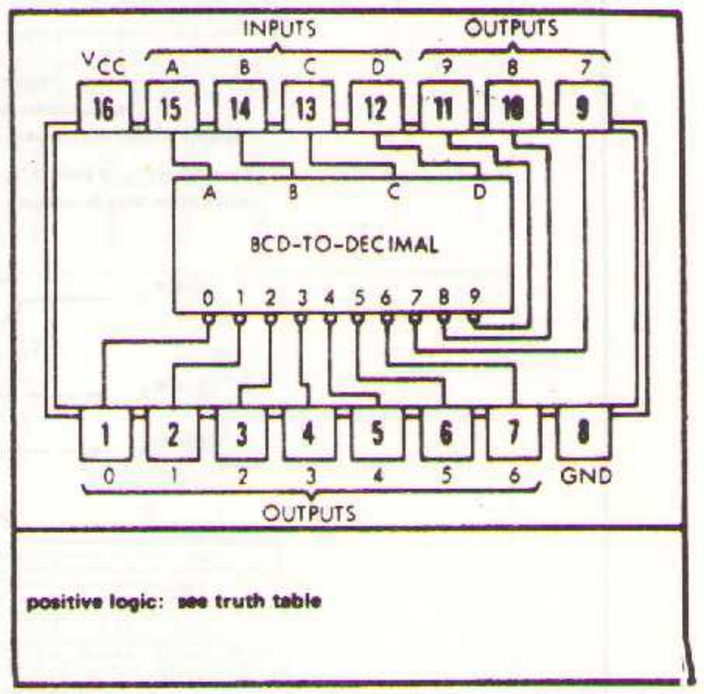
- Full Decoding of Input Logic
- 80 mA Sink-Current Capability

logic

TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	1	1	1	1	1	1	1	1	1
0	0	0	1	1	0	1	1	1	1	1	1	1	1
0	0	1	0	1	1	0	1	1	1	1	1	1	1
0	0	1	1	1	1	1	0	1	1	1	1	1	1
0	1	0	0	1	1	1	1	0	1	1	1	1	1
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	1	1	1	1	1	1	0	1	1	1
0	1	1	1	1	1	1	1	1	1	1	0	1	1
1	0	0	0	1	1	1	1	1	1	1	1	0	1
1	0	0	1	1	1	1	1	1	1	1	1	1	0
1	0	1	0	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	1	1	1	1	1	1	1	1	1

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

†Pin assignments for these circuits are the same for all packages.

description

These monolithic BCD-to-decimal decoder/drivers consist of eight inverters and ten four-input NAND gates. The inverters are connected in pairs to make BCD input data available for decoding by the NAND gates. Full decoding of valid BCD input logic ensures that all outputs remain off for all invalid binary input conditions. These decoders feature TTL inputs and high-performance, n-p-n output transistors designed for use as indicator/relay drivers or as open-collector logic-circuit drivers. Each of the high-breakdown output transistors (SN5445, SN7445 = 30 volts and SN54145, SN74145 = 15 volts) will sink up to 80 milliamperes of current. Each input is one normalized Series 54/74 load. Inputs and outputs are entirely compatible for use with TTL or DTL logic circuits, and the outputs are compatible for interfacing with most MOS integrated circuits. Power dissipation is typically 215 milliwatts.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage, V_{in} (See Note 1)	5.5 V
Maximum Current into each Output (See Note 2)	1 mA
Operating Free-Air Temperature Range: SN5445, SN54145 Circuits	−55°C to 125°C
SN7445, SN74145 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. This rating applies when the output is off.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5445, SN54145 Circuits	4.5	5	5.5	V
SN7445, SN74145 Circuits	4.75	5	5.25	V
Voltage on any Output (See Note 2): SN5445, SN7445 Circuits			30	V
SN54145, SN74145 Circuits			15	V

electrical characteristics over recommended operating temperature range (unless otherwise noted)

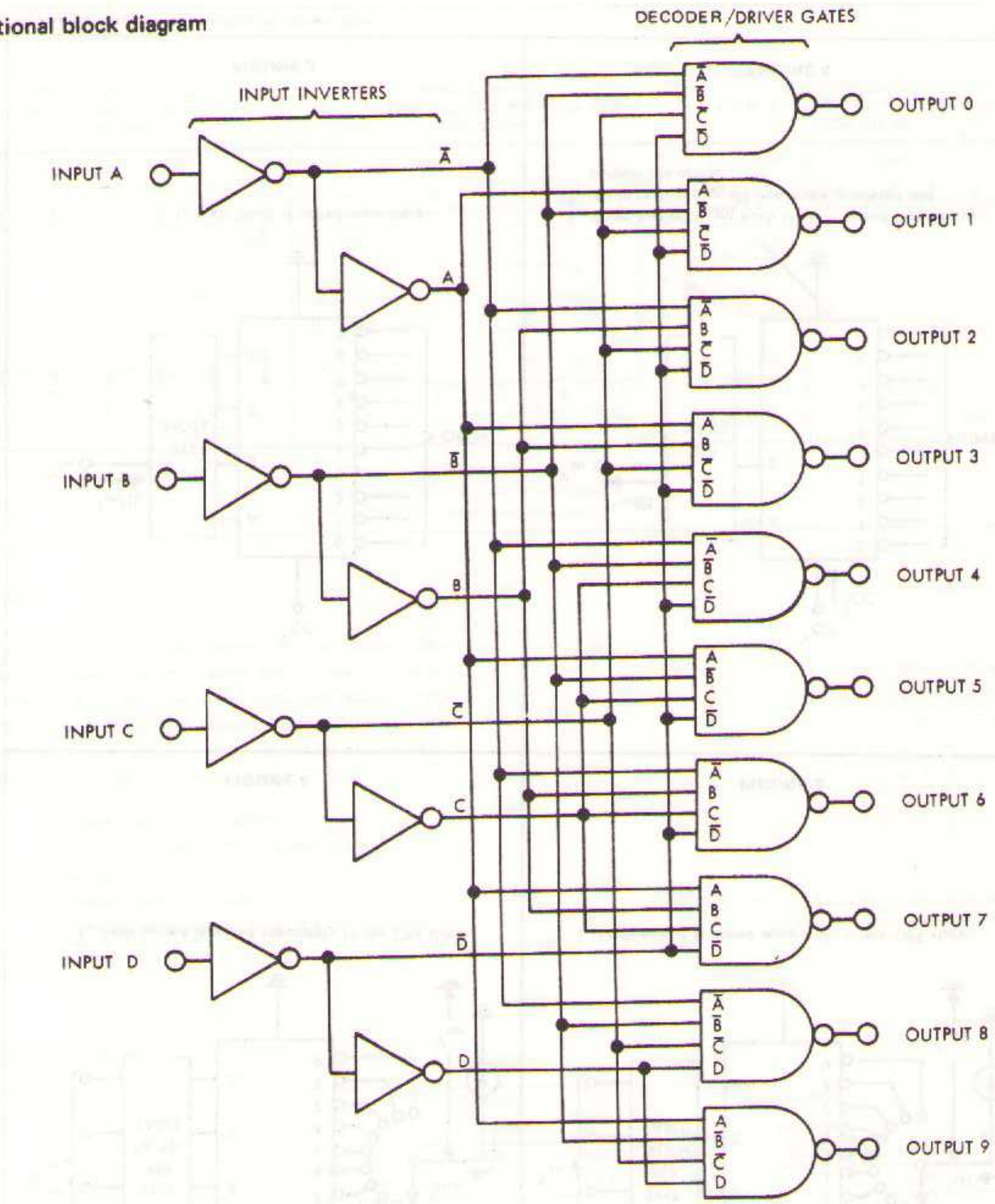
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
V_{on}	On-state output voltage	1	V_{CC} = MIN,	I_{sink} = 80 mA		0.5	0.9	V
			V_{CC} = MIN,	I_{sink} = 20 mA			0.4	V
V_{off}	Off-state output voltage (SN5445 or SN7445)	2	V_{CC} = MAX,	I_{off} = 250 μA	30			V
V_{off}	Off-state output voltage (SN54145 or SN74145)	2	V_{CC} = MAX,	I_{off} = 250 μA	15			V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	4	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
I_{CC}	Supply current	4	V_{CC} = MAX	SN5445, SN54145		43	62	mA
				SN7445, SN74145		43	70	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

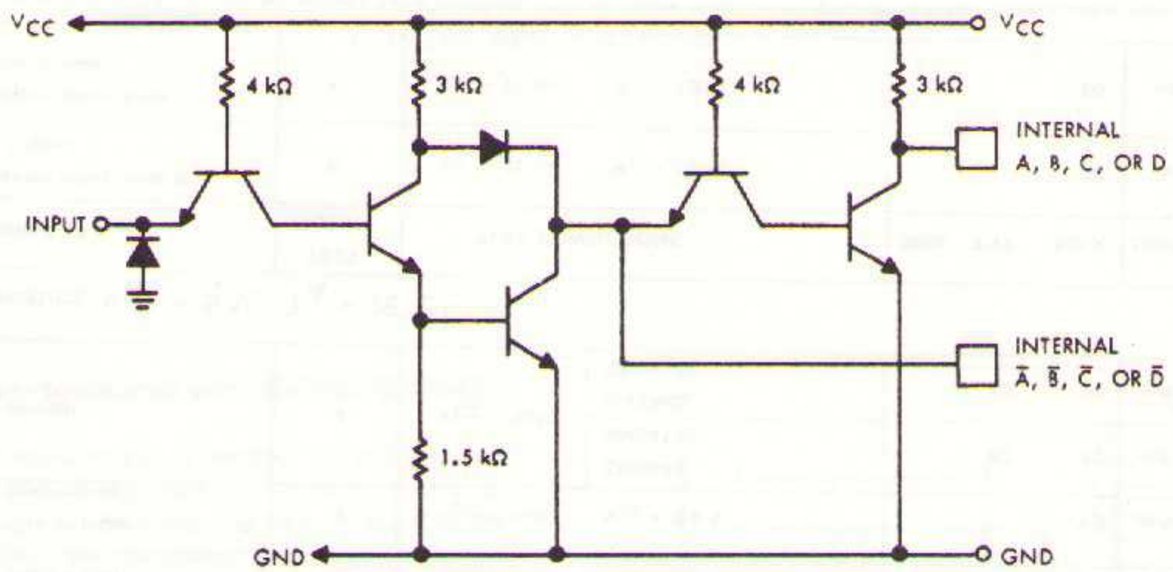
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Propagation delay time to logical 1 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns
t_{pd0}	Propagation delay time to logical 0 level	5	C_L = 15 pF, R_L = 100 Ω			50	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

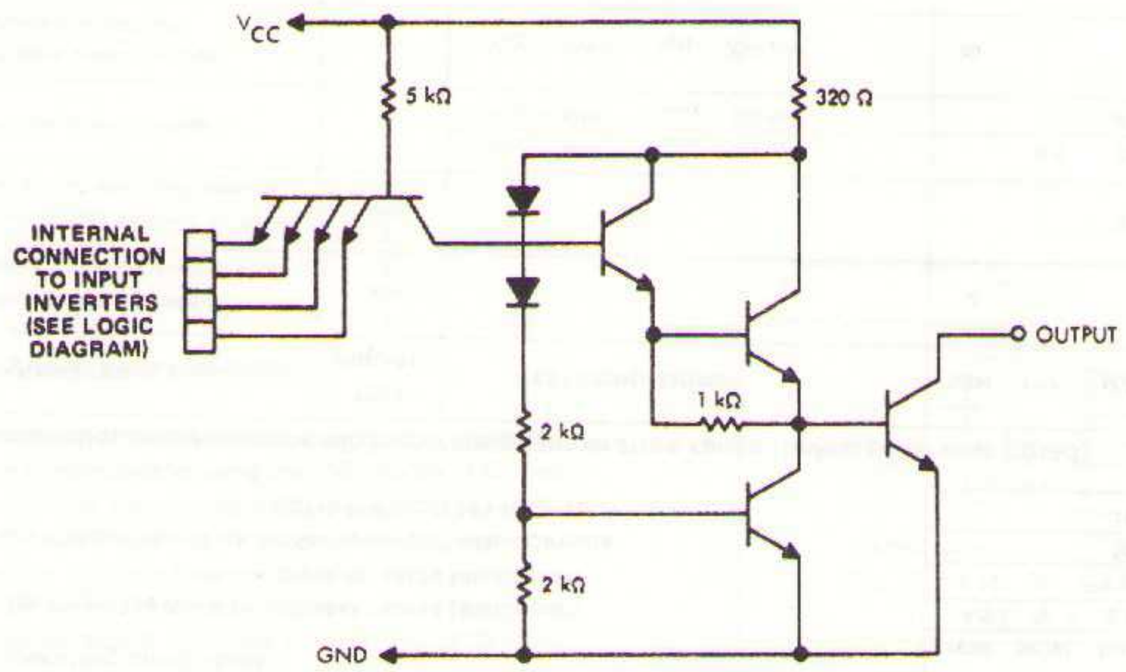
functional block diagram



schematic



EACH PAIR OF INPUT INVERTERS

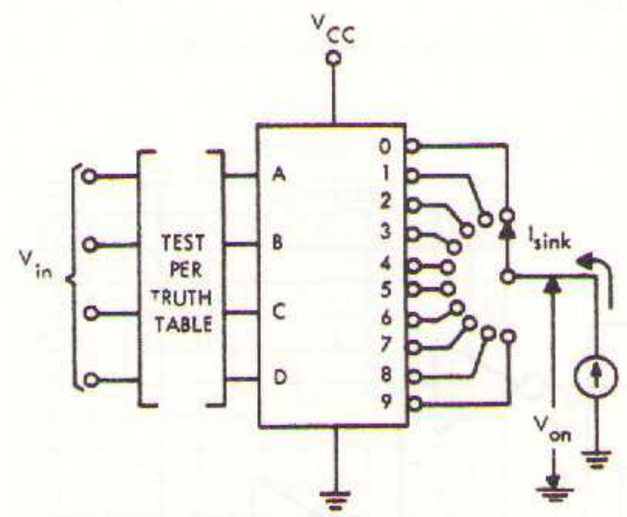


EACH DECODER/DRIVER GATE

NOTE: 1. Component values shown are nominal.

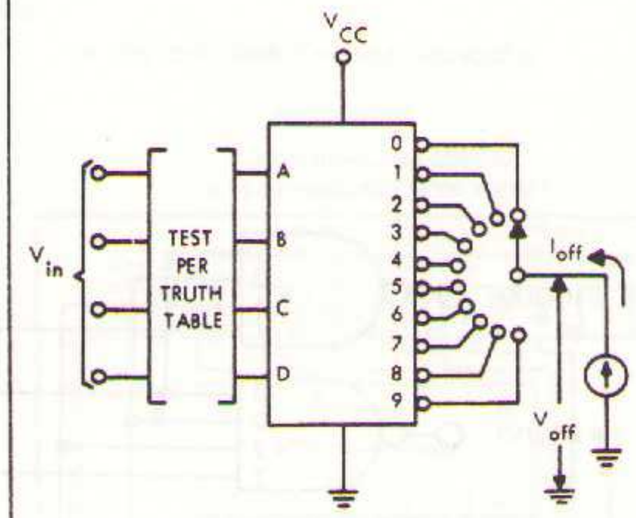
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



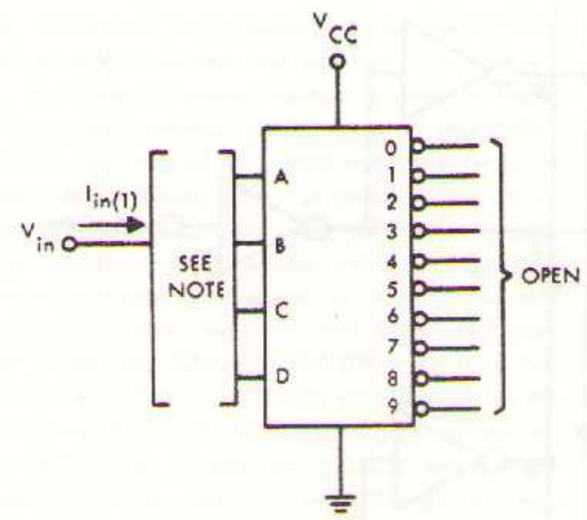
1. Each output is tested separately in the ON state.

FIGURE 1



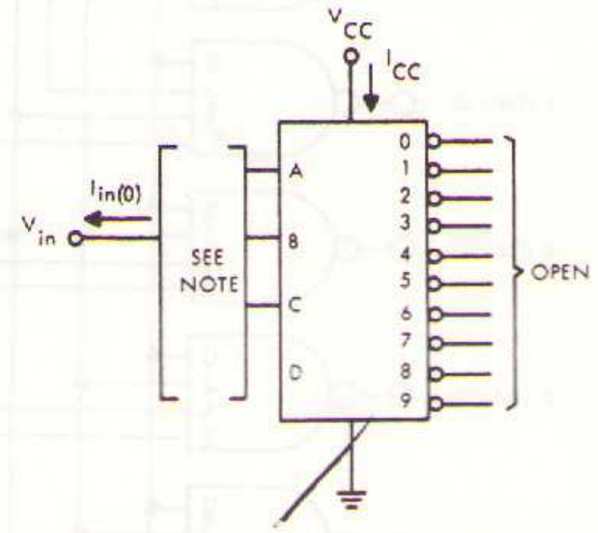
1. Each output is tested separately in the OFF state.

FIGURE 2



1. Each input is tested separately.

FIGURE 3



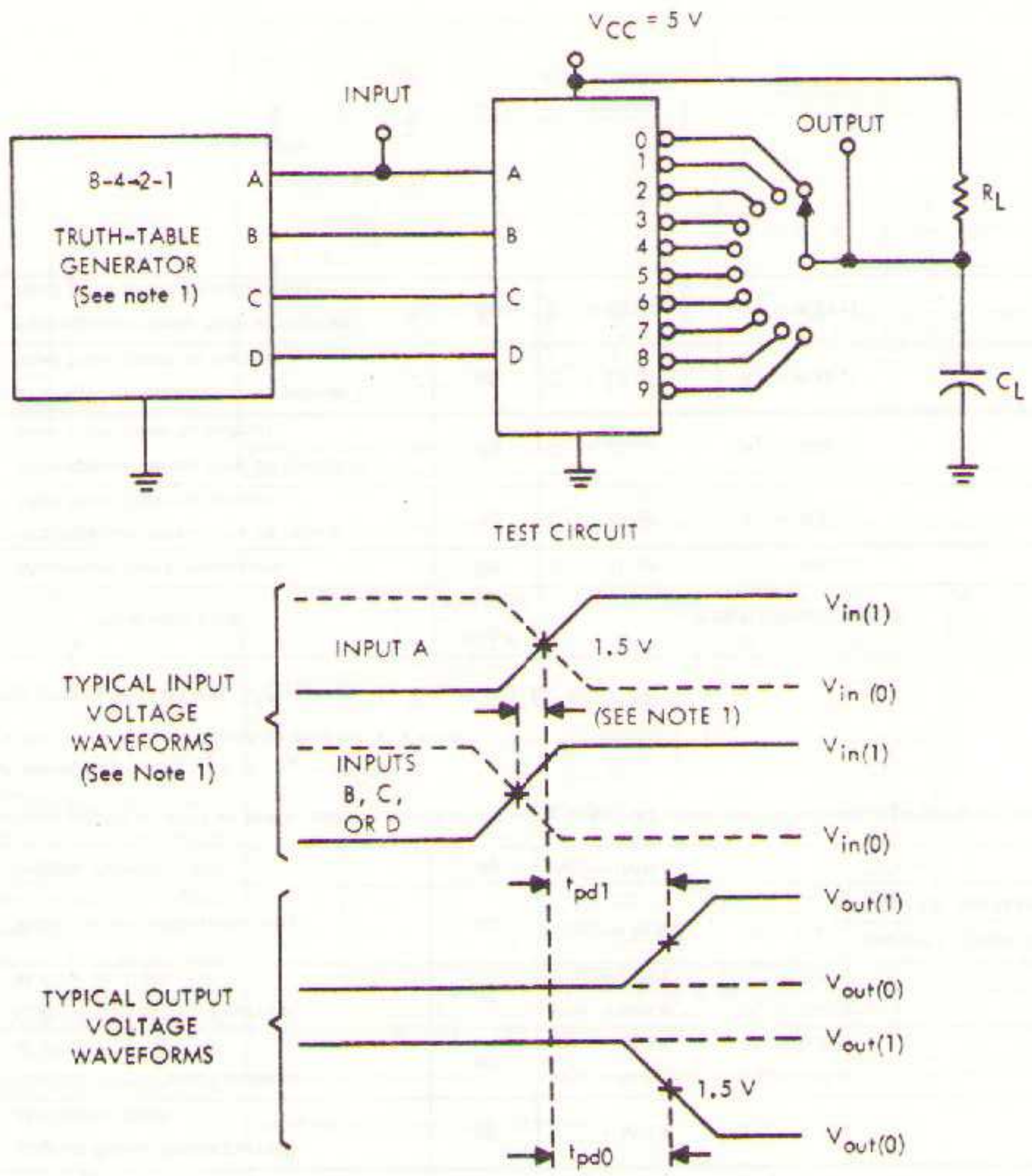
1. When testing $I_{in(0)}$ each input is tested separately.
2. When testing I_{CC} all inputs are grounded and outputs are open.

FIGURE 4

† Arrows indicate actual direction of current flow

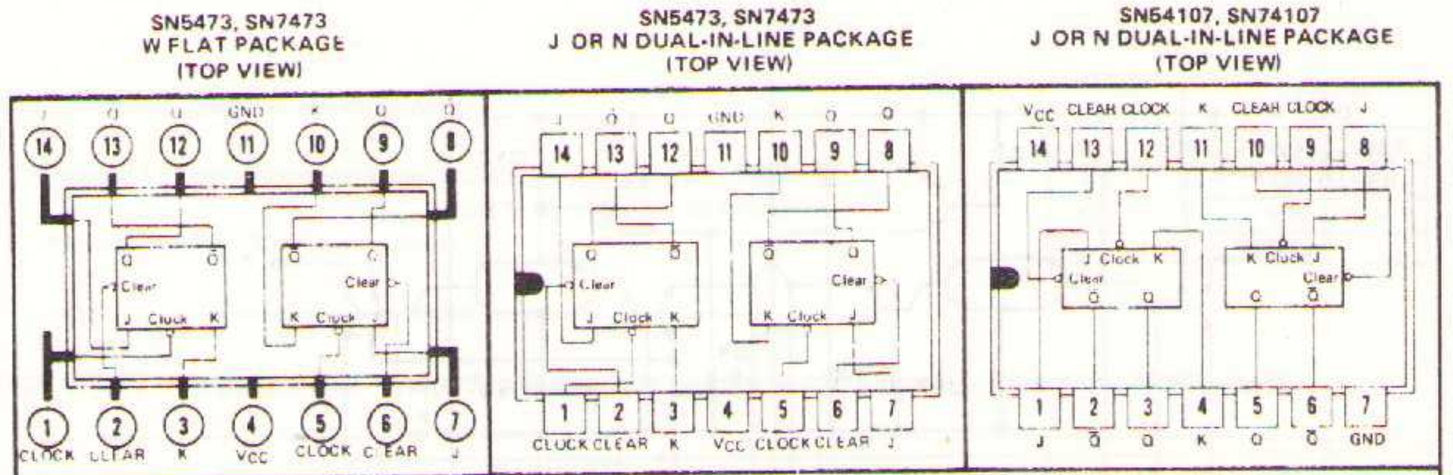
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The truth-table generator has the following characteristics: $V_{out(1)} \geq 2.4$ V, $V_{out(0)} \leq 0.4$ V, t_r and $t_f < 10$ ns, and PRR = 1 MHz. Inputs B, C, and D transitions occur simultaneously with or prior to input A transitions.
2. C_L includes probe and jig capacitance.

FIGURE 5-SWITCHING TIMES



positive logic:
Low input to clear sets Q to logical 0.
Clear is independent of clock.

description

These J-K flip-flops are based on the master-slave principle. Inputs to the master section are controlled by the clock pulse. The clock pulse also regulates the state of the coupling transistors which connect the master and slave sections. The sequence of operation is as follows: (See waveform on page 2-26)

1. Isolate slave from master
2. Enter information from J and K inputs to master
3. Disable J and K inputs
4. Transfer information from master to slave.

logic

TRUTH TABLE (Each Flip-Flop)		
t_n		t_{n+1}
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\bar{Q}_n$

NOTES: 1. t_n = Bit time before clock pulse.
2. t_{n+1} = Bit time after clock pulse.

recommended operating conditions

	SN5473 SN54107			SN7473 SN74107			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{p(clock)}$ (See Figure 69)	20			20			ns
Width of clear pulse, $t_{p(clear)}$ (See Figure 70)	25			25			ns
Input setup time, t_{setup} (See Figure 69)	$\geq t_{p(clock)}$			$\geq t_{p(clock)}$			
Input hold time, t_{hold}	0			0			
Operating free-air temperature range, T_A	-55	25	125	0	25	70	°C

electrical characteristics (over recommended operating free-air temperature range unless otherwise noted)

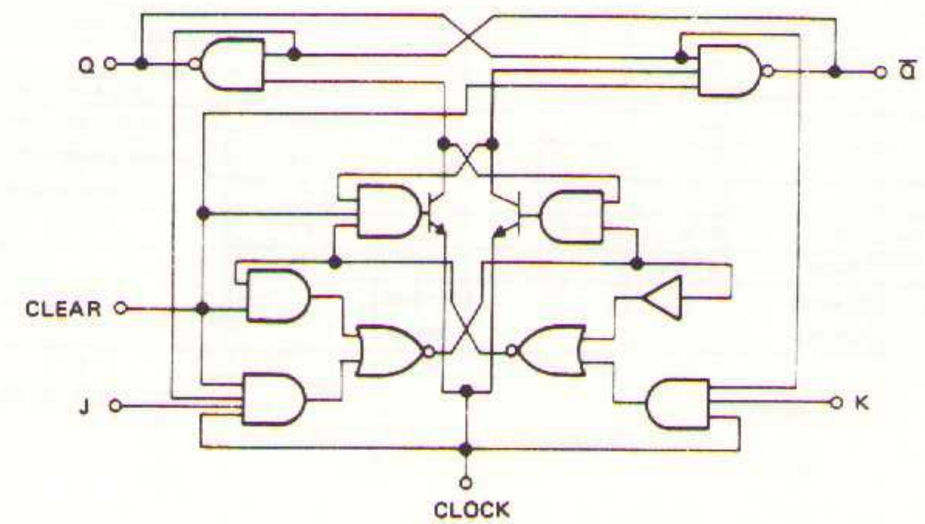
PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	46 and 47				2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	46 and 47						0.8	V
$V_{out(1)}$	Logical 1 output voltage	46	V_{CC} = MIN,	I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	47	V_{CC} = MIN,	I_{sink} = 16 mA			0.22	0.4	V
$I_{in(0)}$	Logical 0 level input current at J or K	48	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at clear or clock	48	V_{CC} = MAX,	V_{in} = 0.4 V				−3.2	mA
$I_{in(1)}$	Logical 1 level input current at J or K	49	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clear or clock	49	V_{CC} = MAX,	V_{in} = 2.4 V				80	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	50	V_{CC} = MAX,	V_{in} = 0	SN5473, SN54107	−20		−57	mA
					SN7473, SN74107	−18		−57	
I_{CC}	Supply current	49	V_{CC} = MAX				20	40	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

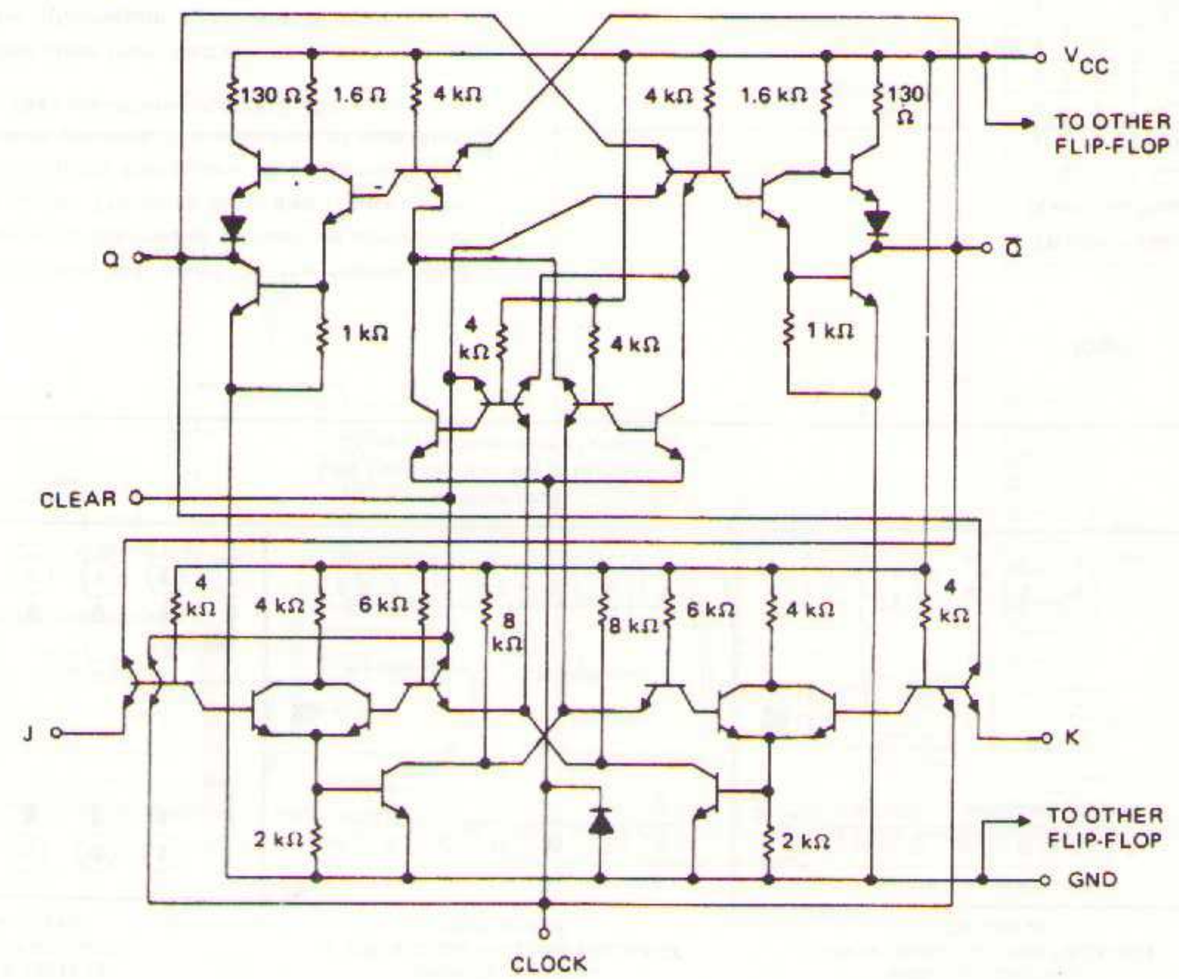
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	69	C_L = 15 pF,	R_L = 400 Ω	15	20		MHz
t_{pd1}	Propagation delay time to logical 1 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	70	C_L = 15 pF,	R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	16	25	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	69	C_L = 15 pF,	R_L = 400 Ω	10	25	40	ns

functional block diagram (each flip-flop)



schematic (each flip-flop)



NOTE: Component values shown are nominal.

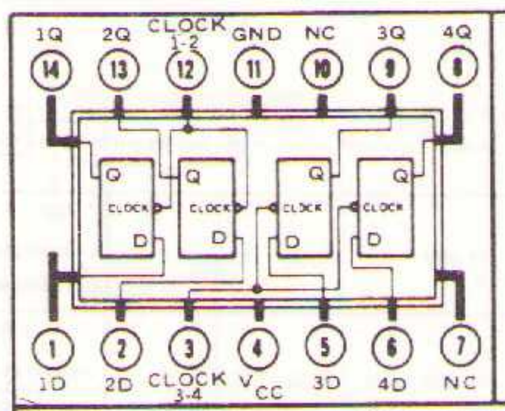
logic

TRUTH TABLE (Each Latch)	
t_n	t_{n+1}
D	Q
1	1
0	0

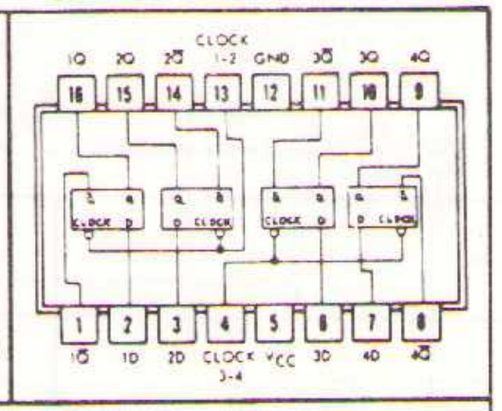
NOTES: 1. t_n = bit time before clock negative-going transition.
2. t_{n+1} = bit time after clock negative-going transition.

NC—No internal connection

SN5477/SN7477
W FLAT PACKAGE
(TOP VIEW)

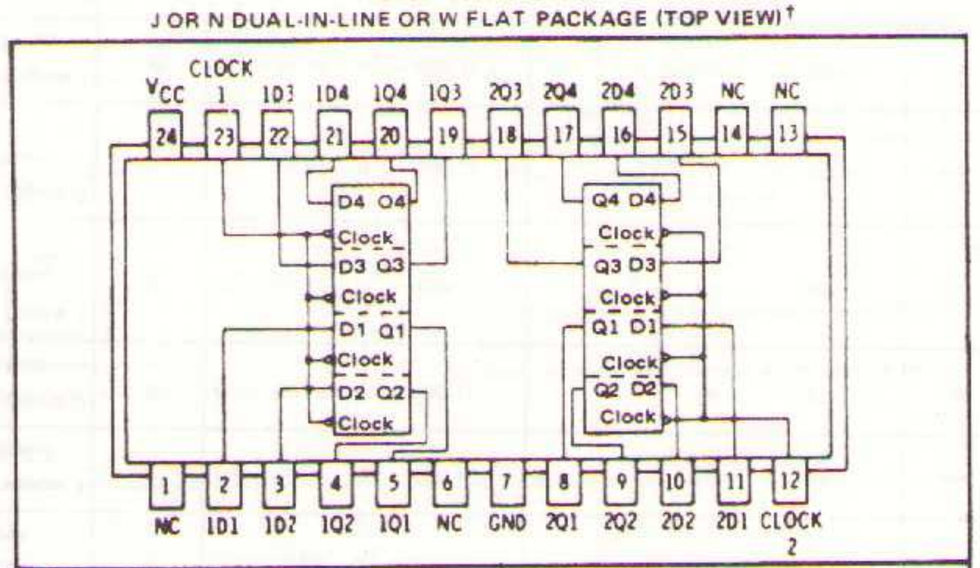


SN5475/SN7475
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

SN54100/SN74100
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see truth table

† Pin assigments for these circuits are the same for all packages

description

These latches are ideally suited for use as temporary storage for binary information between processing units and input/output or indicator units. Information present at a data (D) input is transferred to the Q output when the clock is high, and the Q output will follow the data input as long as the clock remains high. When the clock goes low, the information (that was present at the data input at the time the transition occurred) is retained at the Q output until the clock is permitted to go high.

The SN5475/SN7475 features complementary Q and $\overline{Q}$ outputs from a 4-bit latch, and is available in the 16-pin packages. For higher component density applications the SN5477/SN7477 4-bit latch is available in the 14-pin flat package. The SN54100/SN74100 features two independent quadruple latches in a single 24-pin dual-in-line package.

These circuits are completely compatible with all popular TTL or DTL families. Typical power dissipation is 40 milliwatts per latch. The Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C and Series 74 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage, V_{CC} (See Note 3)		7 V
Input Voltage, V_{in} (See Notes 3 and 4)		5.5 V
Operating Free-Air Temperature Range:	SN5475 Circuits	−55°C to 125°C
	SN7475 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 3. These voltage values are with respect to network ground terminal.
4. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 3): SN5475, SN5477, SN54100	4.5	5	5.5	V
SN7475, SN7477, SN74100	4.75	5	5.25	V
Normalized Fan-Out From Outputs			10	

NOTE: 3. These voltages are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 level at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 level at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 2	V_{CC} = MIN, I_{load} = −400 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 and 2	V_{CC} = MIN, I_{sink} = 16 mA				0.4	V
$I_{in(0)}$	Logical 0 level input current at D	3	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
$I_{in(0)}$	Logical 0 level input current at clock	3	V_{CC} = MAX,	SN5475, SN5477, SN7475, SN7477			−6.4	mA
				SN54100, SN74100			−12.8	mA
$I_{in(1)}$	Logical 1 level input current at D	3	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at clock	3	V_{CC} = MAX, V_{in} = 2.4 V,	SN5475, SN5477, SN7475, SN7477			160	μA
				SN54100, SN74100			320	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX, V_{out} = 0	SN5475, SN5477, SN54100	−20		−57	mA
				SN7475, SN7477, SN74100	−18		−57	mA
I_{CC}	Supply current	5	V_{CC} = MAX,	SN5475, SN5477		32	46	mA
				SN54100		64	92	mA
				SN7475, SN7477		32	53	mA
				SN74100		64	106	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

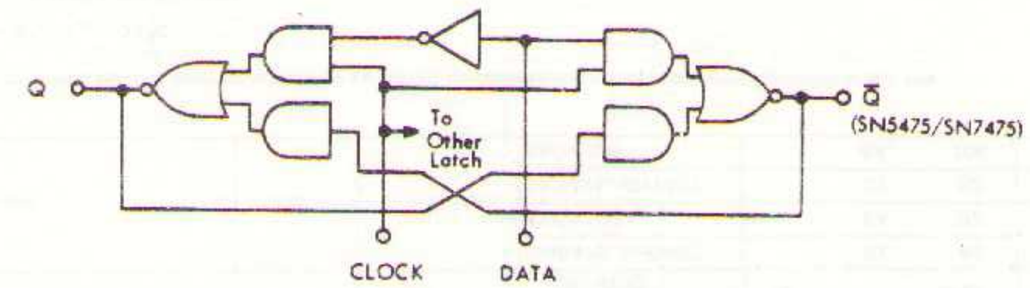
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

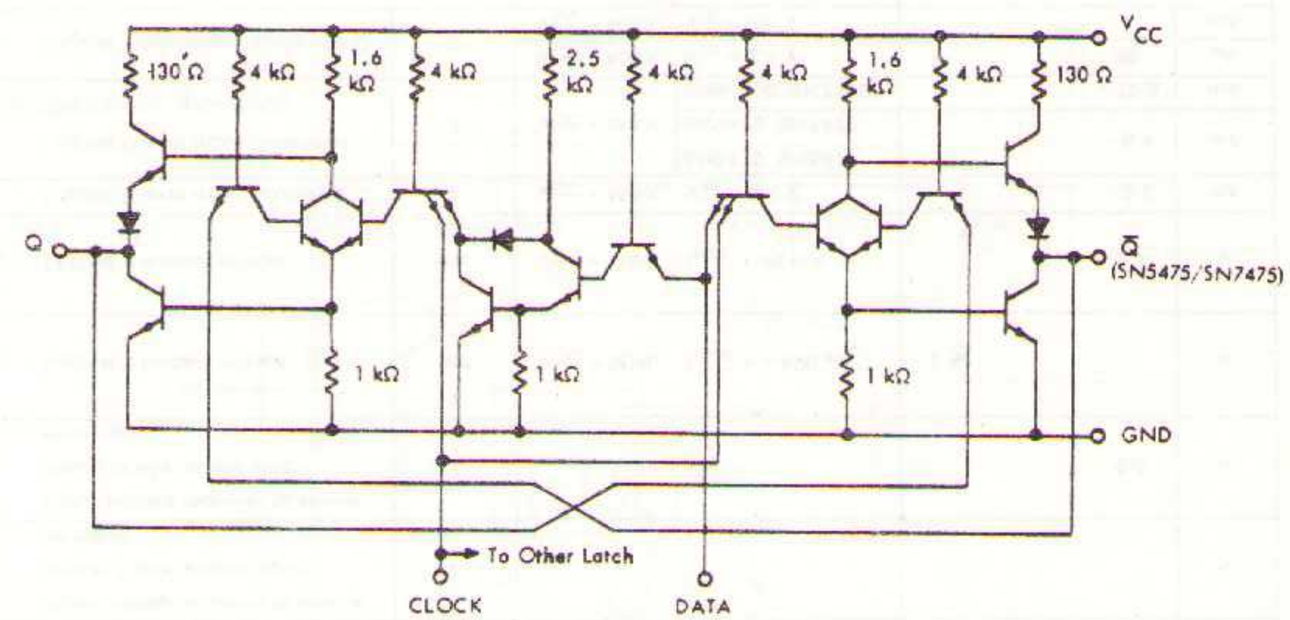
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{setup1}	Minimum logical 1 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		7	20	ns
t_{setup0}	Minimum logical 0 level input setup time at D input	6	C_L = 15 pF, R_L = 400 Ω		14	20	ns
t_{hold1}	Maximum logical 1 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	15¶		ns
t_{hold0}	Maximum logical 0 level input hold time required at D input	6	C_L = 15 pF, R_L = 400 Ω	0	6¶		ns
$t_{pd1(D\text{-}Q)}$	Propagation delay time to logical 1 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(D\text{-}Q)}$	Propagation delay time to logical 0 level from D input to Q output	6	C_L = 15 pF, R_L = 400 Ω		14	25	ns
$t_{pd1(D\text{-}\bar{Q})}$	Propagation delay time to logical 1 level from D input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		24	40	ns
$t_{pd0(D\text{-}\bar{Q})}$	Propagation delay time to logical 0 level from D input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C\text{-}Q)}$	Propagation delay time to logical 1 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C\text{-}Q)}$	Propagation delay time to logical 0 level from clock input to Q output	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns
$t_{pd1(C\text{-}\bar{Q})}$	Propagation delay time to logical 1 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		16	30	ns
$t_{pd0(C\text{-}\bar{Q})}$	Propagation delay time to logical 0 level from clock input to $\bar{Q}$ output (SN5475, SN7475)	6	C_L = 15 pF, R_L = 400 Ω		7	15	ns

¶ These typical times indicate that period occurring prior to the fall of clock pulse (t_0) below 1.5 V when data at the D input will still be recognized and stored.

functional block diagram (each latch)

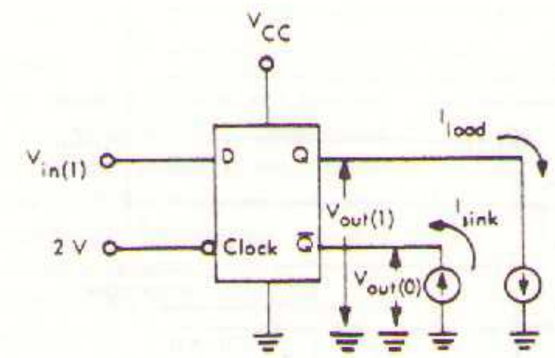


schematic (each latch)



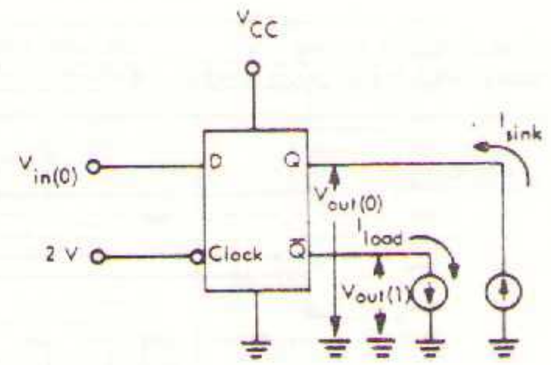
Component values shown are nominal.

d-c test circuits †



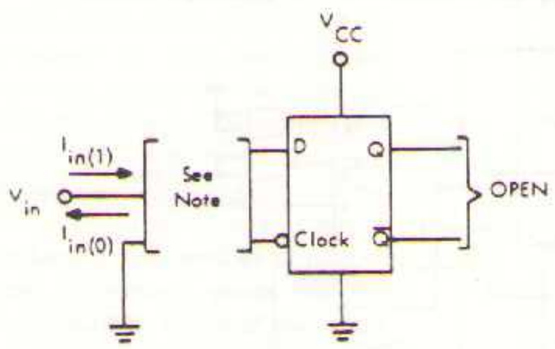
1. Each latch is tested separately.

FIGURE 1



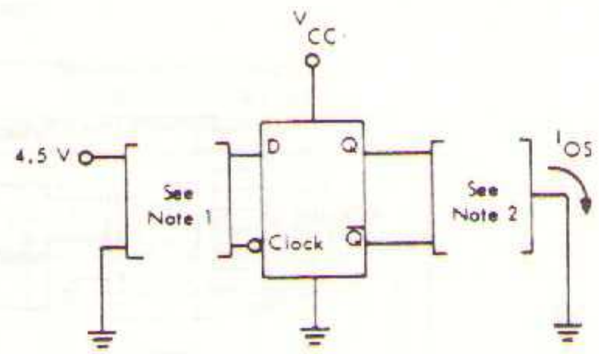
1. Each latch is tested separately.

FIGURE 2



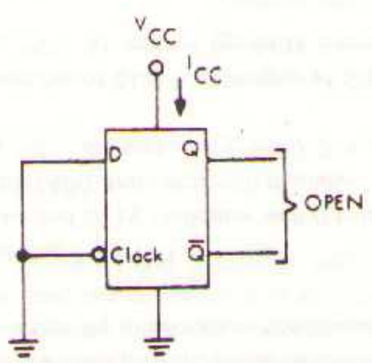
1. Each input is tested separately.
2. When testing $I_{in(1)}$ at D ground clock.
3. When testing $I_{in(1)}$ at clock ground all D inputs.

FIGURE 3



1. Input conditions are in accordance with truth table.
2. Each latch and each output is tested separately.

FIGURE 4

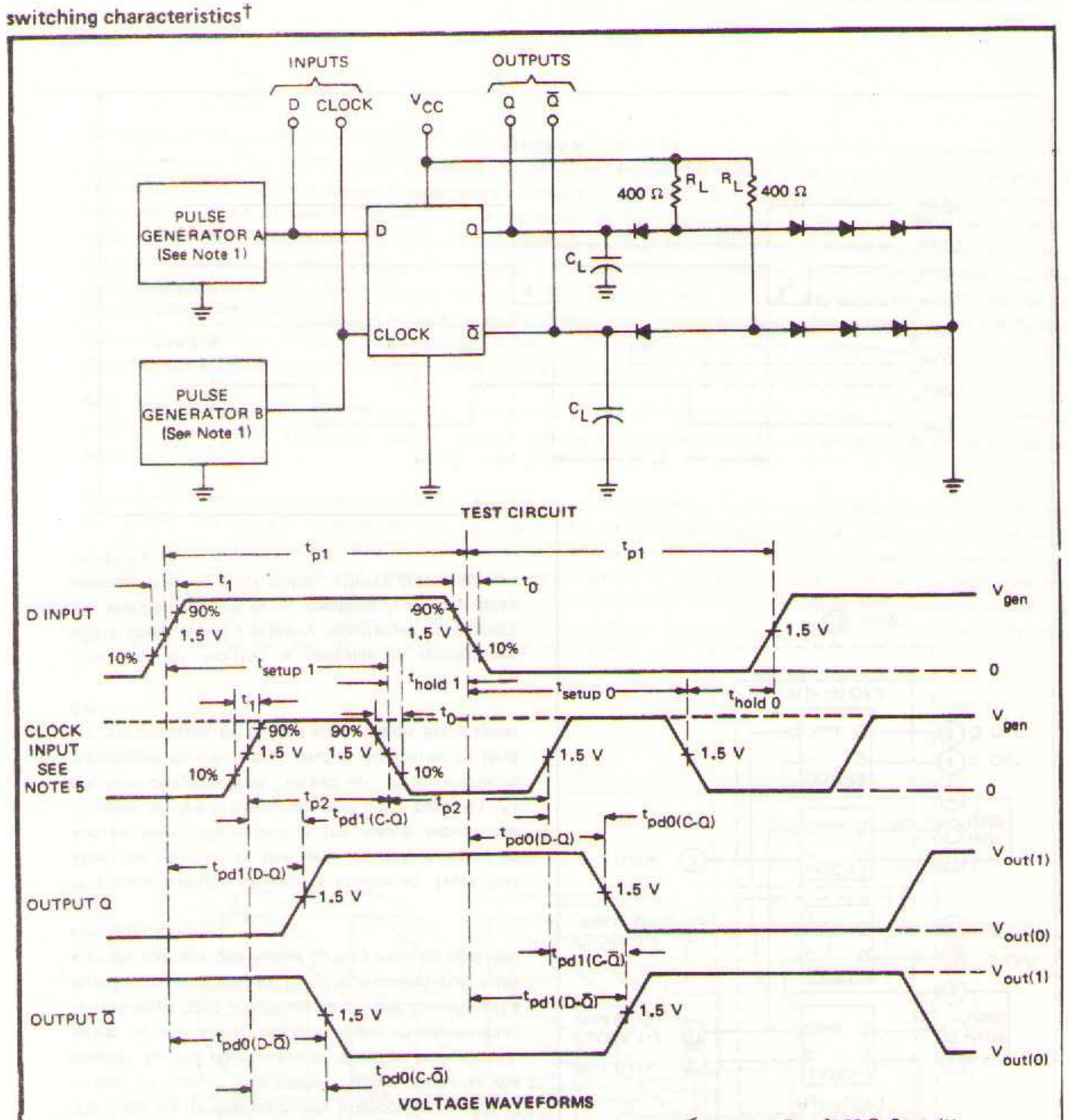


1. All latches are tested simultaneously.

FIGURE 5

† Arrows indicate actual direction of current flow. Complementary $\bar{Q}$ outputs are available on the SN5475/SN7475.

switching characteristics†



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq 10$ ns, and $Z_{out} \approx 50\ \Omega$. For pulse generator A t_{p1} = 1 μs and PRR = 500 kHz. For pulse generator B, t_{p2} = 500 ns and PRR = 1 MHz. Positions of D-input and clock-input pulses are varied with respect to each other to verify setup and hold times.
2. Each latch is tested separately.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.
5. When measuring $t_{pd1(D-Q)}$ and $t_{pd0(D-Q)}$ (or $t_{pd0(D-\bar{Q})}$ and $t_{pd1(D-\bar{Q})}$ for the SN5475/SN7475), clock input must be held at logical 1.

FIGURE 6 – SWITCHING TIMES

†Complementary Q outputs are on the SN5475/SN7475 only.

TYPICAL APPLICATION

temporary storage of binary data

This application demonstrates the use of the SN7475 bistable latch as a temporary storage of binary-coded decimal data, from the SN7490 decade counter, which is to be decoded by the SN7441 decoder/driver. Temporary storage is desirable at this point for two reasons:

a. At counting frequencies above several cycles per second, it is sometimes desirable to eliminate the flicker on the display tube caused by reading an input count which is too fast to be recognized.

b. During the time that the latch is storing information the decade counter may start acquiring data for the next display.

A typical sequence of operation is illustrated (see Figure 7):

1. During t_1, reset decade counter to 0. At end of t_1, indicator will display "0".
2. During t_2, count BCD 3 at output of SN7490. Indicator still displays "0".
3. At start of t_3, indicator will display "3". At end of t_3, BCD 3 is committed to memory by SN7475 and the SN7490 may begin counting again.
4. During t_4, reset decade counter to 0 and count BCD 5 at output of SN7490. Indicator still displays "3".
5. At start of t_5, indicator will display "5". At end of t_5, BCD 5 is committed to memory by SN7475 and the SN7490 is released.

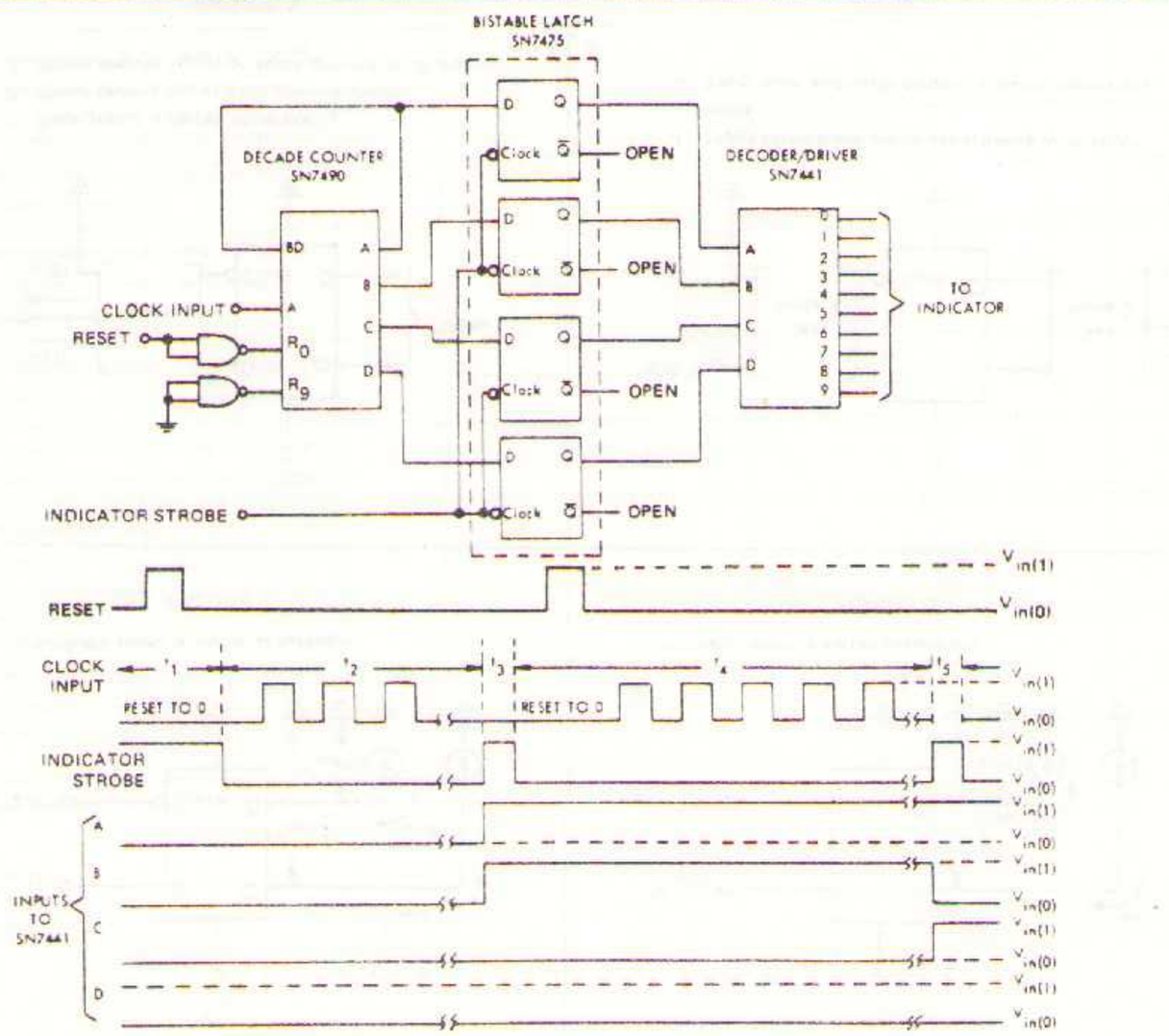


FIGURE 7

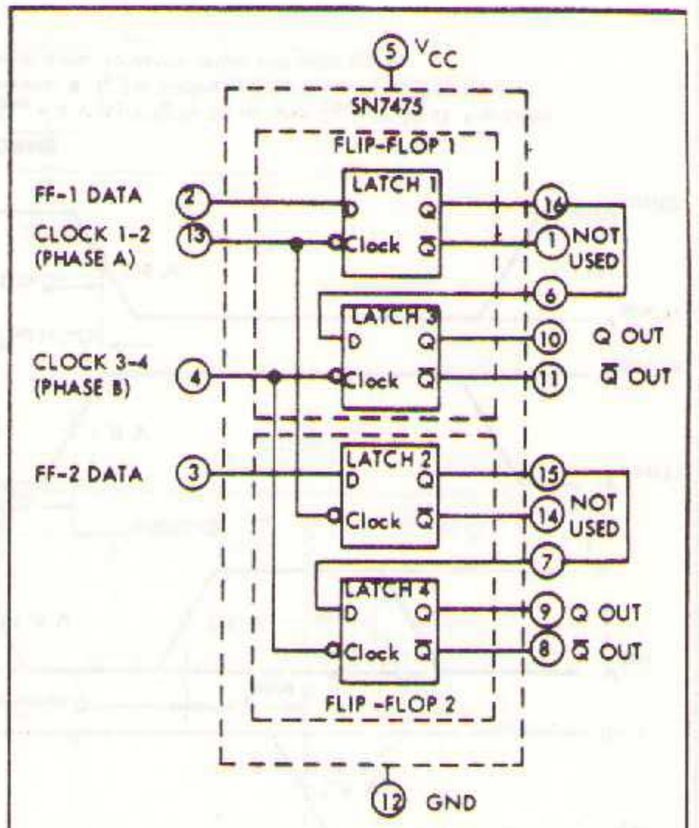
TYPICAL APPLICATION

dual D-type master-slave flip-flop

This application demonstrates the use of the SN7475 as a dual D-type master-slave flip-flop, provided that two-phase clocking is permissible. Each of the D-type flip-flops are formed by merely interconnecting the Q output of one of the latches (which serves as the master) to the data input of another latch (which serves as the slave). Each of these interconnected latches must have a separate clock line; therefore if a dual D-type master-slave flip-flop is constructed from a single package (see Figure 8) they must be operated synchronously.

A typical transfer of data is illustrated. Note that after the start of t_1 the data input is released to acquire new information as the master section has "locked up" the original data after clock pulse A_1. At the start of t_2 the data "locked up" in the master is transferred to the output, and at the end of t_2 (and for the duration of t_3) the slave retains the original data.

This type of flip-flop is desirable in applications where speed is not a primary requirement and where the additional clock skew, resulting from this delay between the two clock pulses, affords greater system reliability.



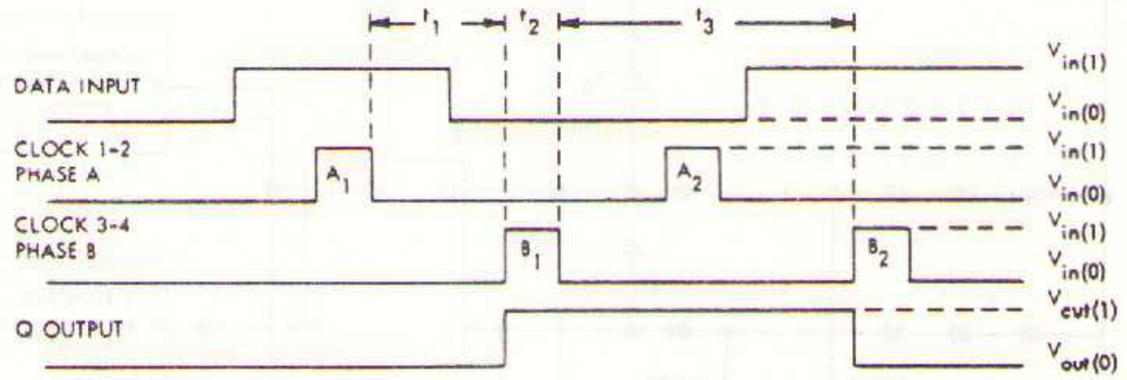


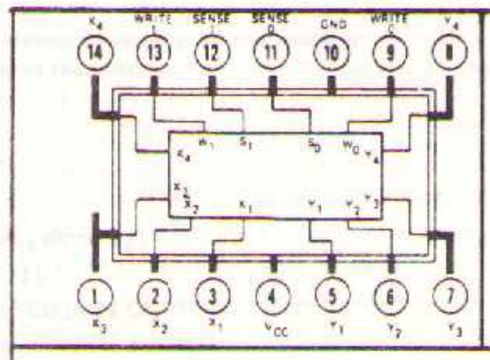
FIGURE 8

description

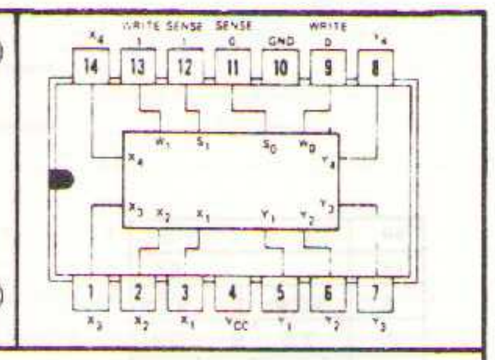
The 16-bit active-element memory is a monolithic, high-speed, transistor-transistor-logic (TTL) array of 16 flip-flops, and two write amplifiers interconnected to form a "scratch-pad" memory with direct-address and non-destructive read-out.

The flop-flops are arranged in a 4-by-4 matrix with each flip-flop representing one bit of 16 words. Four X-address lines and four Y-address lines permit the address of one bit at a time. Each flip-flop, composed of two cross-coupled 3-emitter transistors, is used to store one bit. To determine if a logical 1 or 0 has been stored, it is necessary to know which one of the two flip-flop transistors is conducting. One emitter of each of these transistors serves as the sensing output. All 16 of the logical 1 sensing outputs are connected to the sense logic 1 (S_1) amplifier input and all 16 of the logical0 sensing outputs are connected to the sense logical 0 (S_0) amplifier input. The two remaining emitters on each transistor are used to complete the matrix connections necessary for the X- and Y-address lines. Address line inputs are normally held low (logical 0) and currents from all conducting flip-flop transistors flow out these address lines.

SN5481/SN7481 CIRCUITS
W FLAT PACKAGE (TOP VIEW)

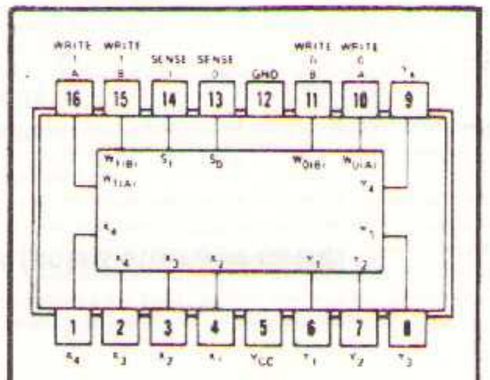


SN5481/SN7481 CIRCUITS
J OR N DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see logic diagram

SN5484/SN7484 CIRCUITS
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see logic diagram

†Pin assignments for these circuits are the same for all packages.

To address a flip-flop both the X- and Y-address lines associated with that flip-flop are taken to a logical 1 voltage. Due to the matrix nature of the circuit, at least one address line of all flip-flops except the one being addressed will continue to remain at a logical 0 level and no change will occur on those flip-flops. But, in the addressed flip-flop, the current in the conducting transistor diverts from the address lines to the appropriate sense line and then to one of the sense amplifiers. Thus, either the sense amplifier associated with a logical 1 or the sense amplifier associated with a logical 0 is activated. When this occurs, the output of the activated sense amplifier drops from a logical 1 to a logical 0 level. The memory is non-destructive as the states of the flip-flops are not disturbed during sensing. The memory is volatile and information will be lost if the supply voltage is removed.

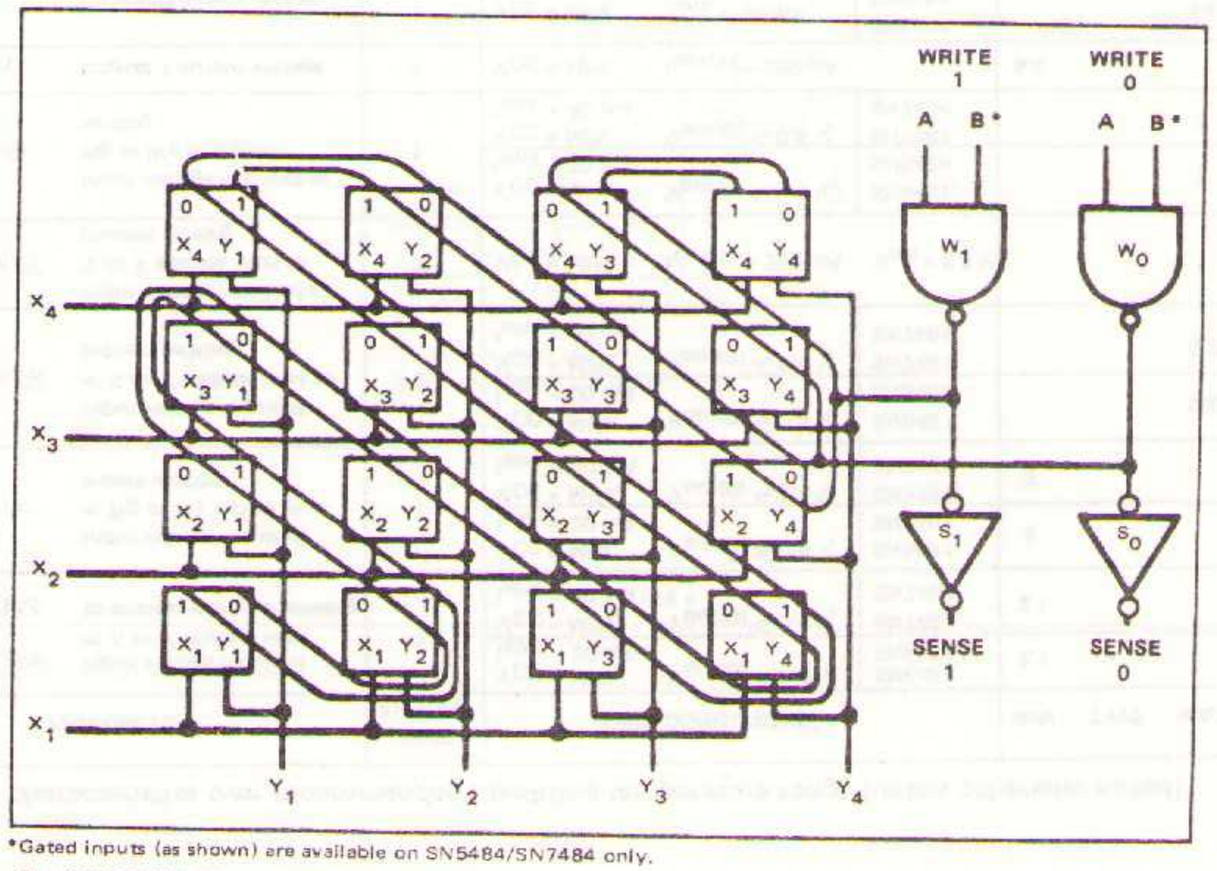
description (continued)

To store new information in a flip-flop, it is necessary to address it and apply logical 1 voltage to the appropriate write amplifier input. (The SN5484/SN7484 circuit has gated write-amplifier inputs). The output of the write amplifier responds by dropping to a logical 0 level. Since all logical 0 sense lines are connected to the output of the logical 0 write amplifier and all logical 1 sense lines are connected to the output of the logical 1 write amplifier, a logical 0 voltage on the output of a write amplifier will apply the same voltage to emitters of all flip-flop transistors connected to that amplifier. In all flip-flops except the one being addressed, this low voltage has no effect since at least one other emitter on each of the flip-flop transistors is held low by the address lines. But two possibilities exist with the flip-flop that is addressed. The flip-flop may already be in the desired state, in which case no change occurs. But if the flip-flop must be changed from one state to the other, the low voltage applied to the emitter of the transistor which is not conducting turns that transistor on causing the other transistor to turn off.

Since the connection between the output of the write amplifier and the sense line is common to the input of the sense amplifier, the memory cannot be used to provide information on the state of a bit while the write amplifiers are activated.

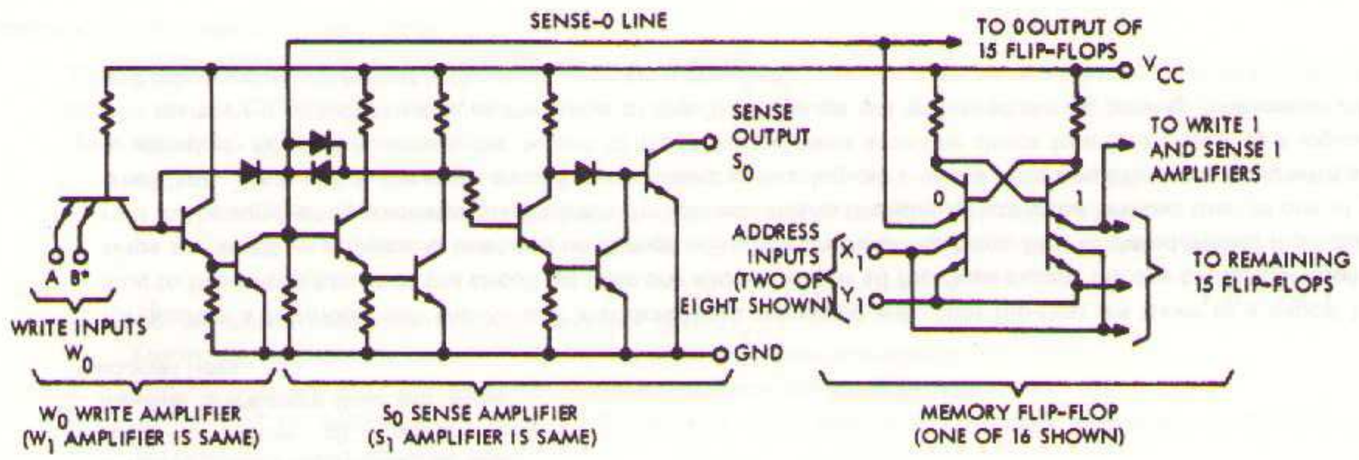
A number of active element memories may be paralleled to form the desired matrix size (number of words) and to form the desired word length (number of bits). Standard TTL circuitry, employed for the address line inputs, write amplifier inputs, and the saturating output transistors, provides complete TTL and DTL compatibility and maintains typical noise margins of one volt. Average power dissipation is 275 milliwatts (typical), and the open-collector outputs may be wire-OR connected to similar outputs. Internal circuitry of the write and sense amplifiers are operated within their linear range to improve speed. Sensing propagation delay times are typically 20 nanoseconds when operated at full fan-out and 30 picofarads of circuit capacitance.

logic diagram



*Gated inputs (as shown) are available on SN5484/SN7484 only.
The SN5481/SN7481 has one W_0 and one W_1 input.

schematic diagram



* Gated inputs (as shown) are available on SN5484/SN7484 only. The SN5481/SN7481 has one W_0 and one W_1 input.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)	7 V
Input Voltage V_{in} (See Notes 1 and 2)	5.5 V
Operating Free-Air Temperature Range: SN5481, SN5484 Circuits	−55°C to 125°C
SN7481, SN7484 Circuits	0°C to 70°C
Storage Temperature Range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5481, SN5484 Circuits	4.5	5	5.5	V
SN7481, SN7484 Circuits	4.75	5	5.25	V
Width of Write Pulse, $t_{p(write)}$ (See Figure 11)	25			ns
Address Lines Input Setup Time, t_{setup} (See Figure 11)	0			ns

NOTES: 1. These voltage values are with respect to ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
$V_{in(1)AW}$ or $V_{in(1)AS}$	Input voltage required at X or Y address lines to ensure writing or sensing	1	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484	2.1			V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484	2.1			V
$V_{in(1)W}$	Input voltage required at W_0 or W_1 inputs to ensure writing	1	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484	2			V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484	2			V
$V_{in(0)A\overline{W}}$	Input voltage required at X or Y address lines to prevent writing	2	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484			0.8	V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484			0.8	V
$V_{in(0)A\overline{S}}$	Input voltage required at X or Y address lines to prevent sensing	3	V_{CC} = MIN,	$I_{out(1)}$ = 250 μA	V_{out} = 5.5 V			1	V
$V_{in(0)\overline{W}}$	Input voltage required at W_0 or W_1 to prevent writing	1	V_{CC} = MIN, I_{sink} = 20 mA	$V_{out(0)} \leq 0.4$ V,	SN5481, SN5484			1	V
			V_{CC} = MIN, I_{sink} = 40 mA	$V_{out(0)} \leq 0.4$ V,	SN7481, SN7484			1	V
$V_{out(1)}$	Logical 1 output voltage	3	V_{CC} = MIN,	$I_{out(1)}$ = 250 μA		5.5			V
$V_{out(0)}$	Logical 0 output voltage (on level)	1 and 2	V_{CC} = MIN,	I_{sink} = 20 mA	SN5481, SN5484			0.4	V
			V_{CC} = MIN,	I_{sink} = 40 mA	SN7481, SN7484			0.4	V
$I_{in(0)}$	Logical 0 level input current at write 1 and write 0 (each input)	4	V_{CC} = MAX,	V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at all X or all Y address lines	5	V_{CC} = MAX,	V_{in} = 0.4 V				−11	mA
$I_{in(1)}$	Logical 1 level input current at write 1 and write 0 (each input)	6	V_{CC} = MAX,	V_{in} = 2.4 V				40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at each X and each Y address line	6	V_{CC} = MAX,	V_{in} = 4.5 V				400	μA
			V_{CC} = MAX,	V_{in} = 5.5 V				3	mA
I_{CC}	Supply current	6	V_{CC} = MAX		SN5481, SN5484		55	78	mA
					SN7481, SN7484		55	91	mA

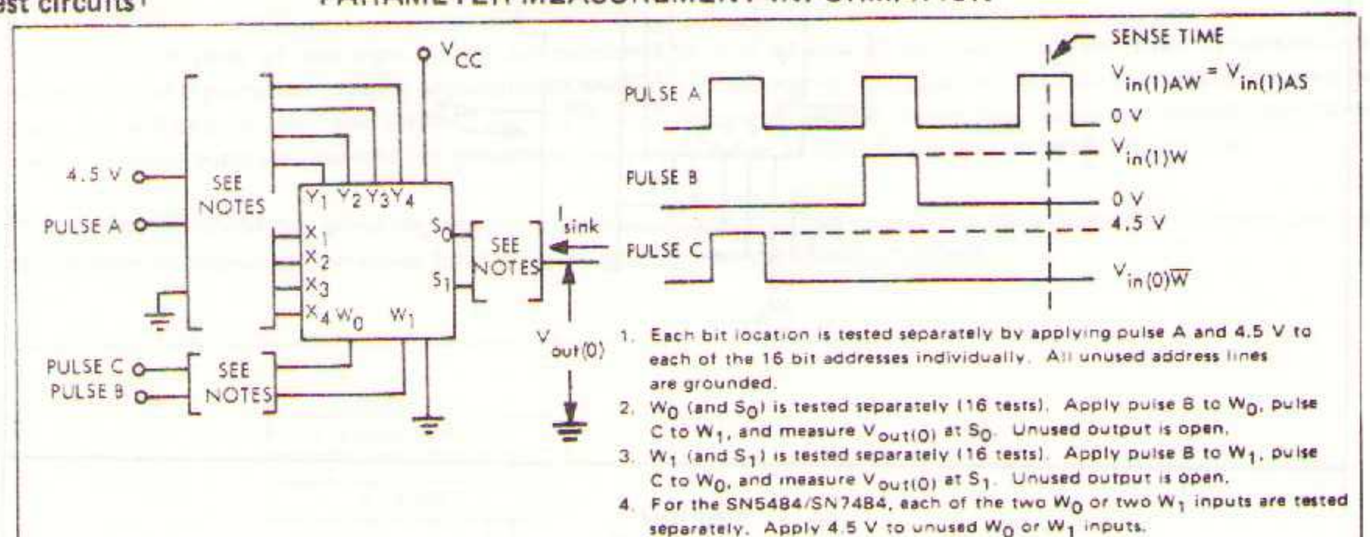
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{WR}	Write recovery time	7	C_L = 15 pF, X_1 - Y_1 location addressed		30	60	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		22	45	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		27	55	ns
t_{pd1}	Propagation delay time to logical 1 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 - Y_1 location addressed		15	25	ns
			C_L = 200 pF, X_1 - Y_1 location addressed		20	35	ns
t_{pd0}	Propagation delay time to logical 0 level from address-line inputs to S_0 or S_1 outputs	7	C_L = 15 pF, X_1 through X_4 and Y_1 locations addressed		20	30	ns

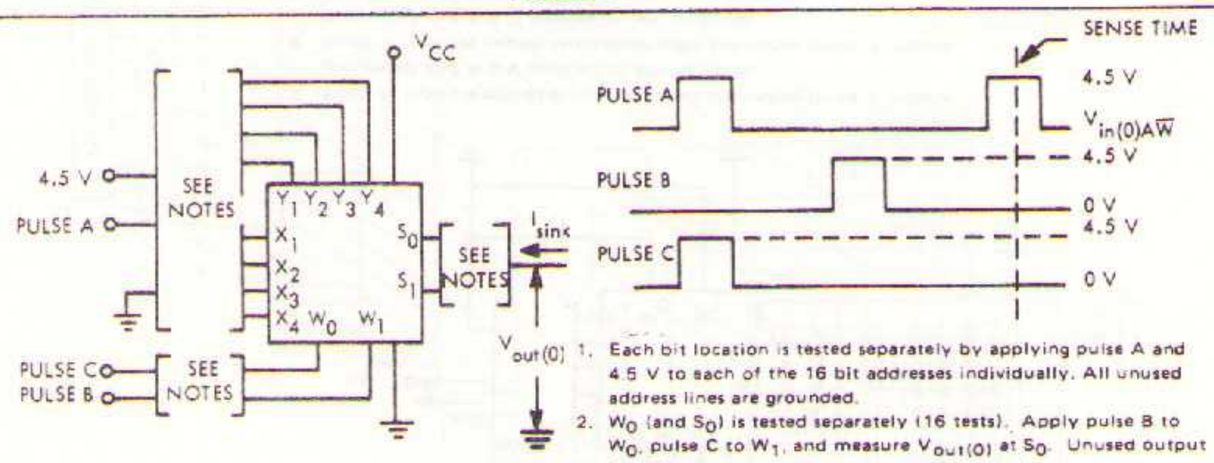
d-c test circuits†

PARAMETER MEASUREMENT INFORMATION



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

FIGURE 1



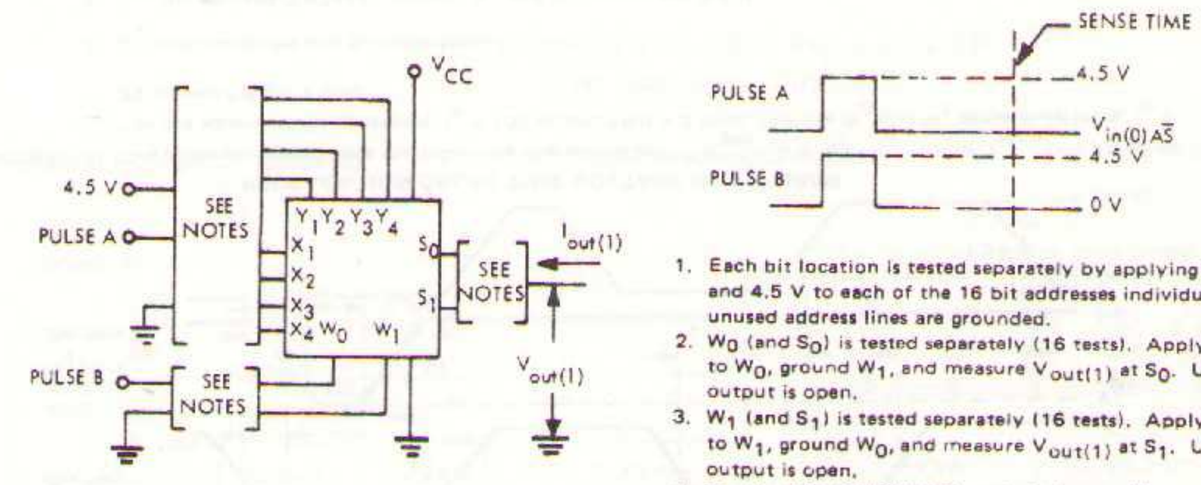
1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, pulse C to W_1, and measure $V_{out(0)}$ at S_0. Unused output is open.
3. W_1 (and S_1) are tested separately (16 tests). Apply pulse B to W_1, pulse C to W_0, and measure $V_{out(0)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to unused W_0 or W_1 inputs.

FIGURE 2

†Arrows indicate actual direction of current flow.

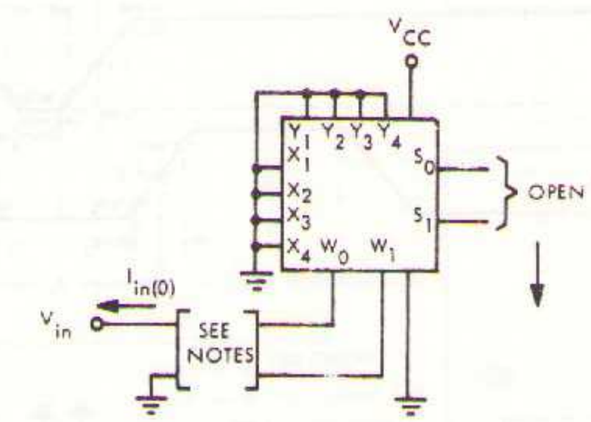
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each bit location is tested separately by applying pulse A and 4.5 V to each of the 16 bit addresses individually. All unused address lines are grounded.
2. W_0 (and S_0) is tested separately (16 tests). Apply pulse B to W_0, ground W_1, and measure $V_{out(1)}$ at S_0. Unused output is open.
3. W_1 (and S_1) is tested separately (16 tests). Apply pulse B to W_1, ground W_0, and measure $V_{out(1)}$ at S_1. Unused output is open.
4. For the SN5484/SN7484, each of the two W_0 or two W_1 inputs are tested separately. Apply 4.5 V to the unused input of the gate under test and ground both inputs of the unused gate.

FIGURE 3



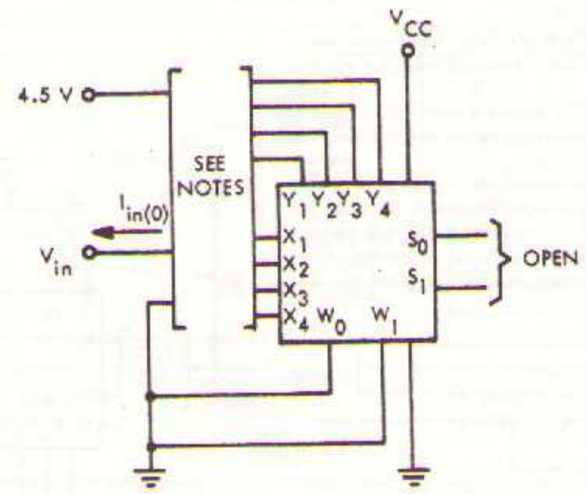
1. Each input is tested separately.
2. All unused inputs are grounded.

FIGURE 4

† Arrows indicate actual direction of current flow.

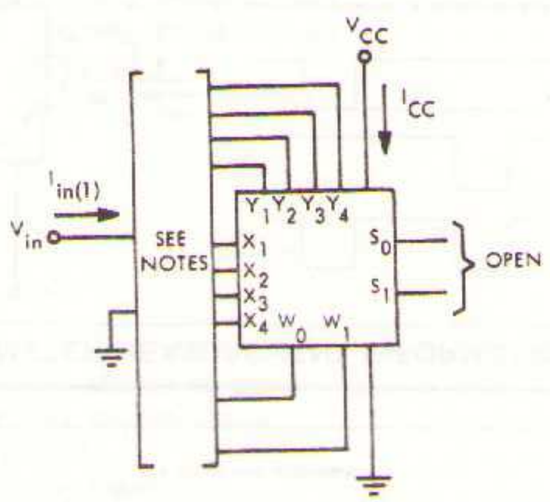
PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



1. Each X input is tested separately with the other three X inputs grounded and 4.5 V applied to all Y inputs.
2. Each Y input is tested separately with the other three Y inputs grounded and 4.5 V applied to all Y inputs.
3. For the SN5484/SN7484, both W_0 and both W_1 inputs are grounded.

FIGURE 5



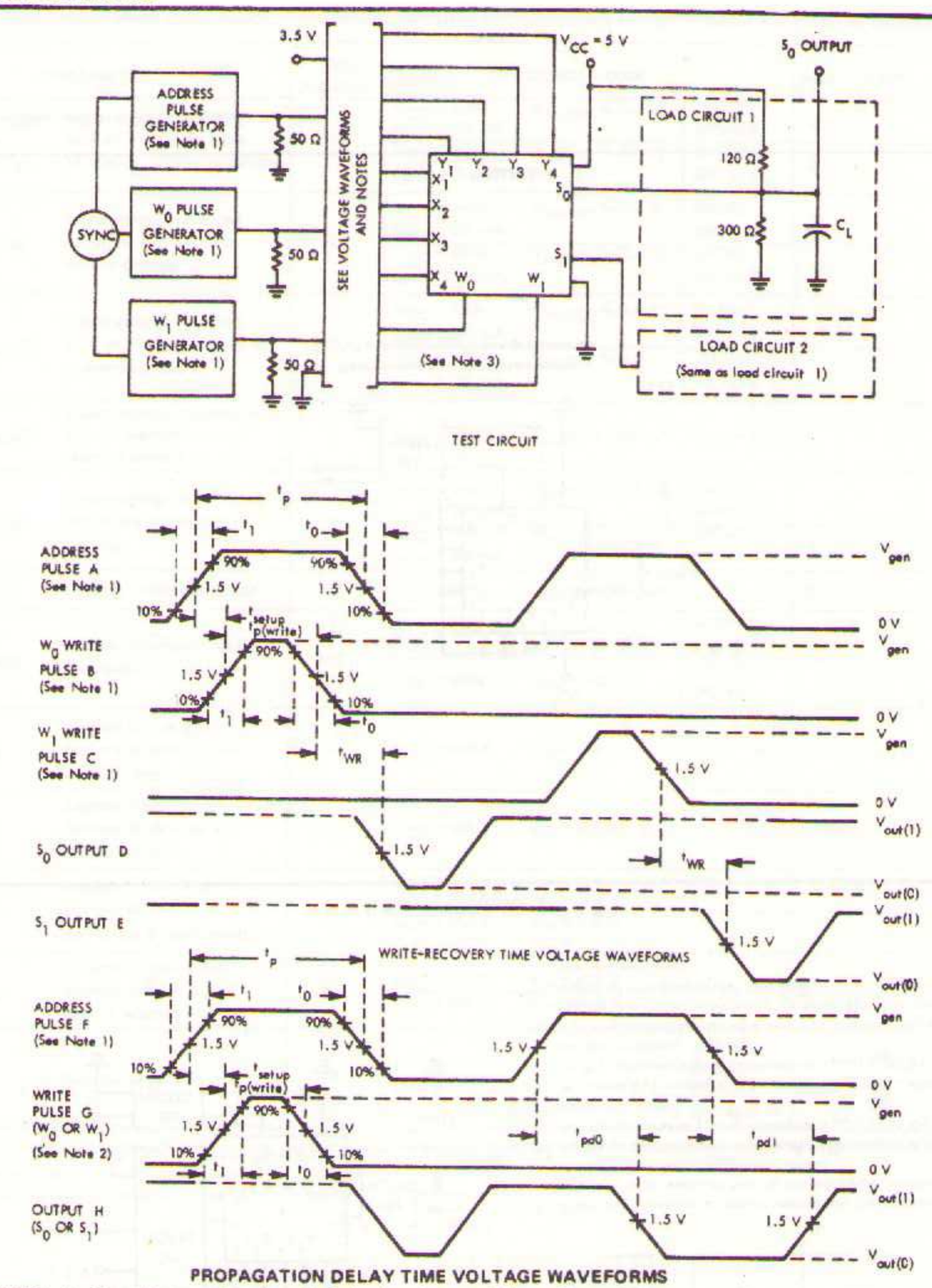
1. Each input is tested separately for $I_{in(1)}$ with all unused inputs grounded.
2. When measuring I_{CC} all inputs are grounded.

FIGURE 6

† Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0$ = 10 ns, t_{setup} = 0 to 10 ns. For the address pulse generator, t_p = 100 ns and PRR = 2 MHz. For the W_0 and W_1 pulse generators, t_p = 25 ns and PRR = 1 MHz.

2. C_L includes probe and jig capacitance.

3. For the SN5484/SN7484, unused W_0 and W_1 inputs are 3.5 V.

FIGURE 7 – SWITCHING CHARACTERISTICS

TYPICAL APPLICATIONS

This application demonstrates use of the 16-bit active element memory to form a high-speed, direct-address, scratch-pad memory having a storage capability of m-words (in multiples of 16) of n-bit length. For purposes of this discussion, a memory is illustrated which will store 64 words each having a length of 8-bits. See Figure A. This storage capability may be increased or decreased using the patterns shown.

In this example, each of the planes consist of four 16-bit memory circuits connected in an 8-by-8 matrix. This organization provides 64 addresses (words) of 8-bits (word length) or a total bit capability of 512 bits (64 X 8).

Each bit plane (B_0 through B_7) is formed by paralleling the W_0, W_1 inputs, S_0, S_1 outputs, and completing the X-Y matrix connections. The matrix is completed by paralleling the X lines of Circuits A-B and C-D and the Y lines of A-C then B-D, to form the 64 addresses of plane B_0. Two pull-up resistors, one for S_0 and one for S_1, should be provided for wired-OR outputs. The other seven planes are identical to B_0.

The X and Y lines of the eight planes are paralleled so that all bits of each word are addressed simultaneously. Addressing of a particular word is accomplished by the X-Y decoder/drivers. For this particular example, the decoder could be a 1-of-8 decoder (see SN7442 and SN7444 applications) and the drivers may consist of discrete transistors, each capable of supplying current for 16 address inputs. A number of decoding/driving schemes are possible.

The SN5484/SN7484 has gated W_0 and W_1 inputs which may be used to perform the write enable function. External gating may be employed if enabling functions are required with the SN5481/SN7481.

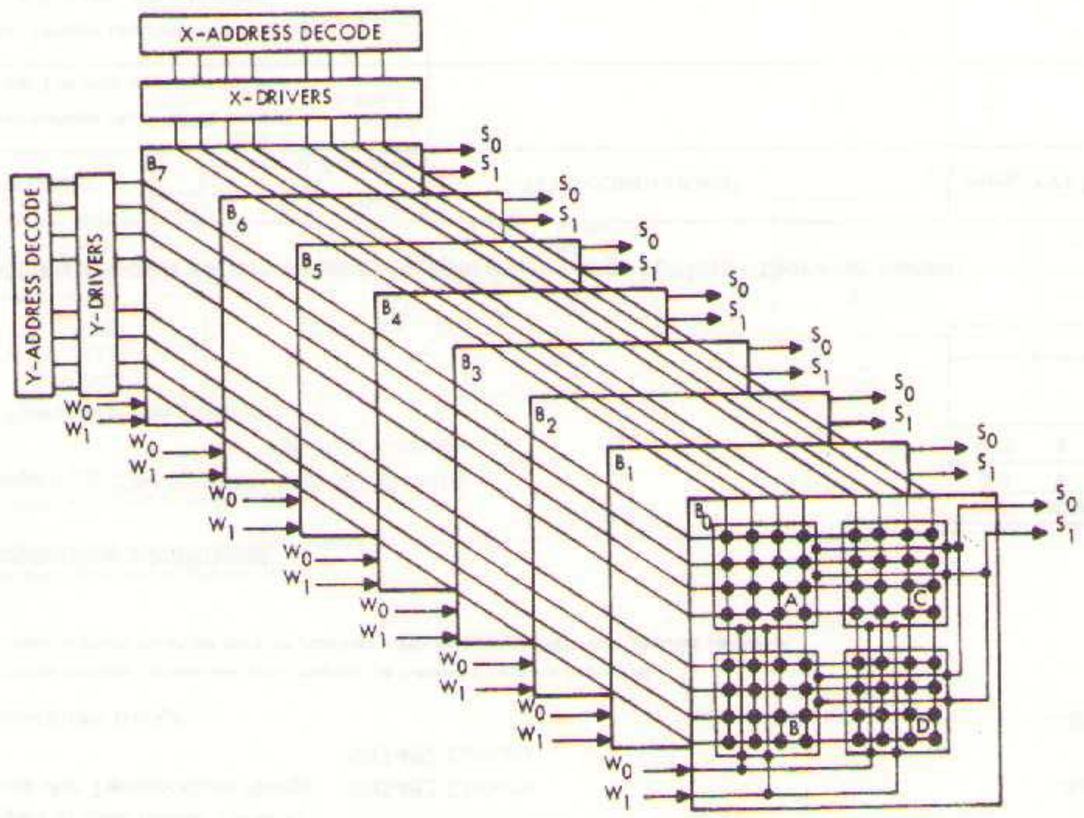


FIGURE A – TYPICAL MEMORY ORGANIZATION

A HIGH-SPEED TTL 2-BIT FULL ADDER FOR APPLICATION IN

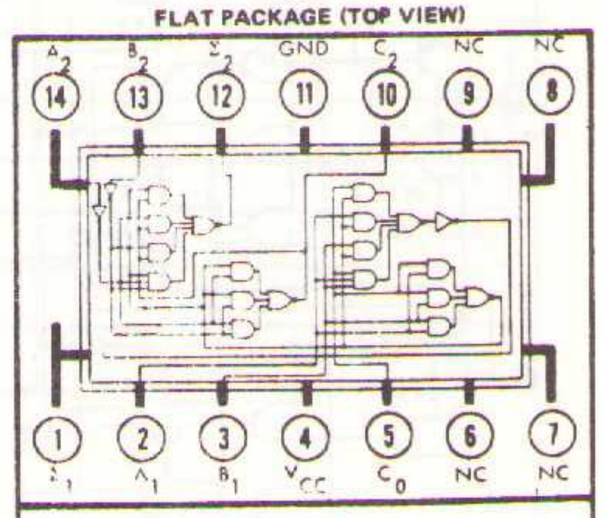
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

TRUTH TABLE

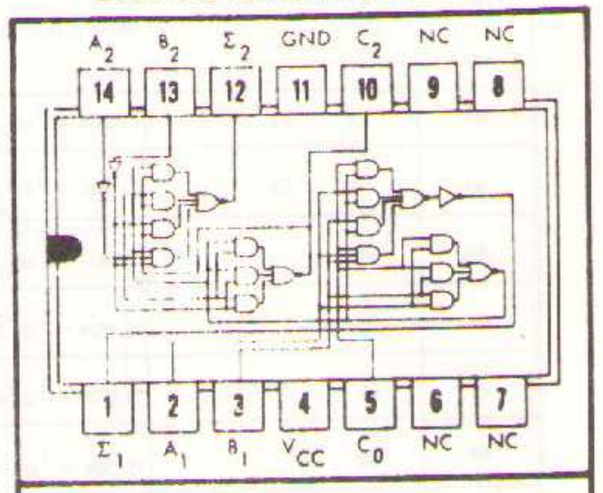
INPUT				OUTPUT					
				WHEN $C_0 = 0$			WHEN $C_0 = 1$		
A_1	B_1	A_2	B_2	Σ_1	Σ_2	C_2	Σ_1	Σ_2	C_2
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

W
FLAT PACKAGE (TOP VIEW)



positive logic: see truth table

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: see truth table

NC No Internal Connection

description

This full adder performs the addition of two 2-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_2) is obtained from the second bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL logic families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform full-adder functions.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Notes 1 and 2) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN5482 Circuits . . . . . −55°C to 125°C
SN7482 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5482 Circuits	4.5	5	5.5	V
SN7482 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:				
C_2			5	
Σ_1 or Σ_2			10	

electrical characteristics over recommended temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4			V
$V_{out(0)}$	Logical 0 output voltage	1					0.4	V
$I_{in(0)}$	*Logical 0 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, B_1, or C_0	3	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at A_2 or B_2	3	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
I_{OS}	Short-circuit output current at Σ_1 or Σ_2§	4	V_{CC} = MAX	SN5482	−20		−55	mA
				SN7482	−18		−55	mA
I_{OS}	Short-circuit output current at C_2§	4	V_{CC} = MAX	SN5482	−20		−70	mA
				SN7482	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX	SN5482		35	50	mA
				SN7482		35	58	mA

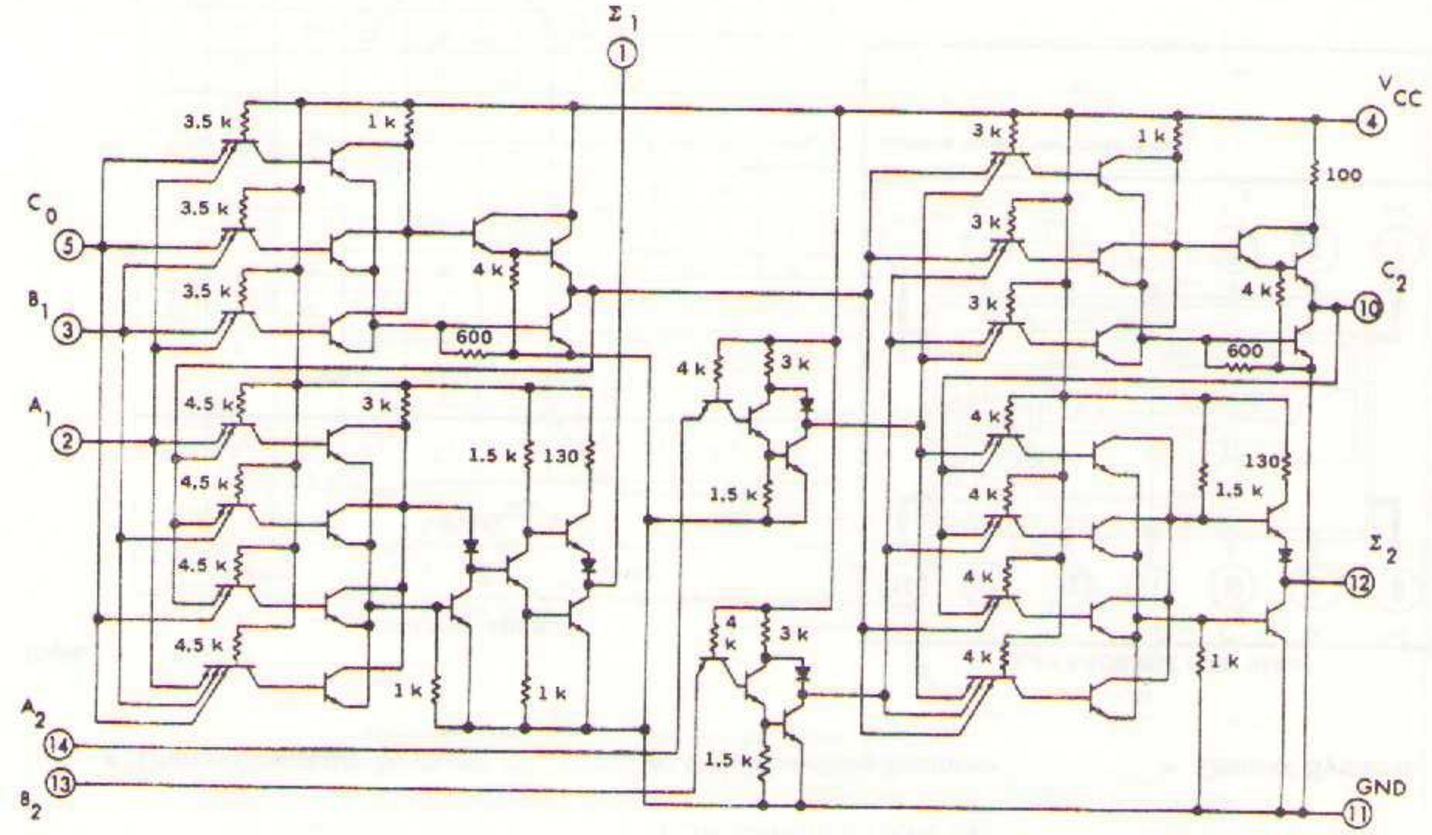
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	Σ_1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	B_2	Σ_2	3	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	C_0	Σ_2	5	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	C_2	7	C_L = 15 pF, R_L = 780 Ω		12	19	ns
t_{pd0}			8	C_L = 15 pF, R_L = 780 Ω		17	27	ns

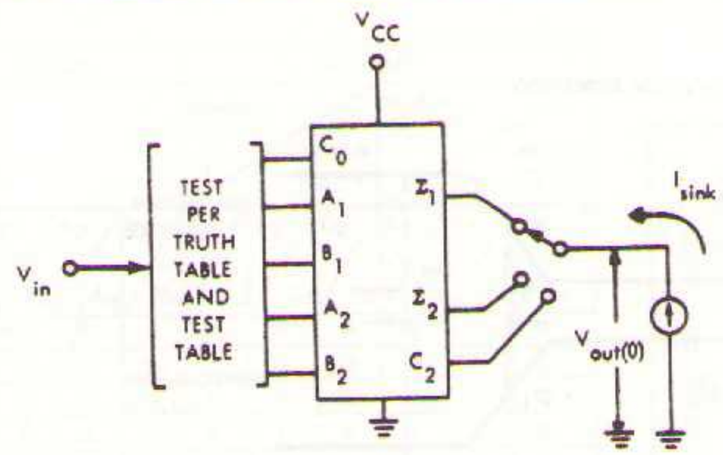
§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

schematic



Component values shown are nominal.
Resistor values are in ohms.

d-c test circuits†

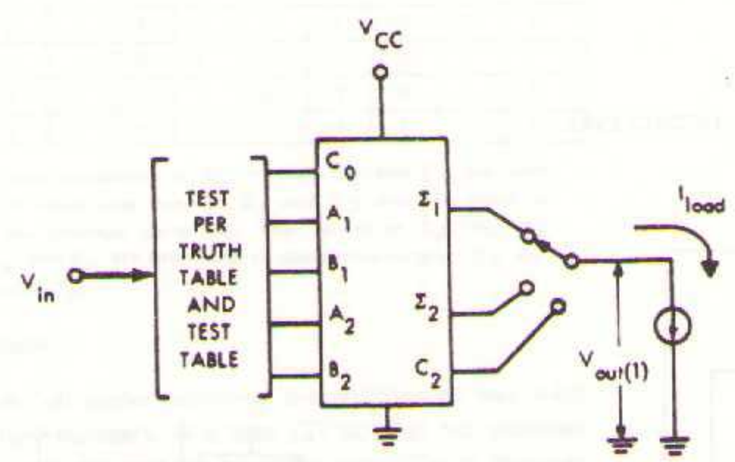


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1 or Σ_2	16 mA
C_2	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

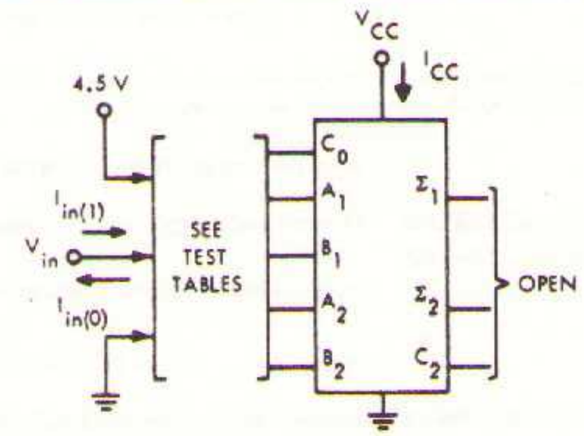
OUTPUT UNDER TEST	I_{load}
Σ_1 or Σ_2	−400 μA
C_2	−200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

d-c test circuits† (continued)



$I_{in(0)}$ TEST TABLE

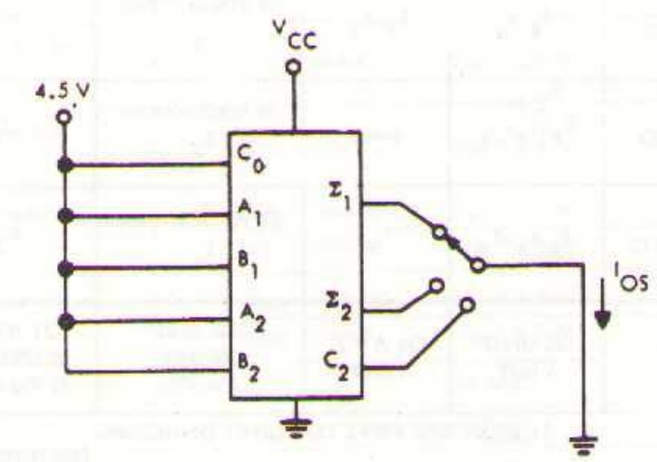
APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None

1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, and C_0; and ground B_1 and B_2.

FIGURE 3



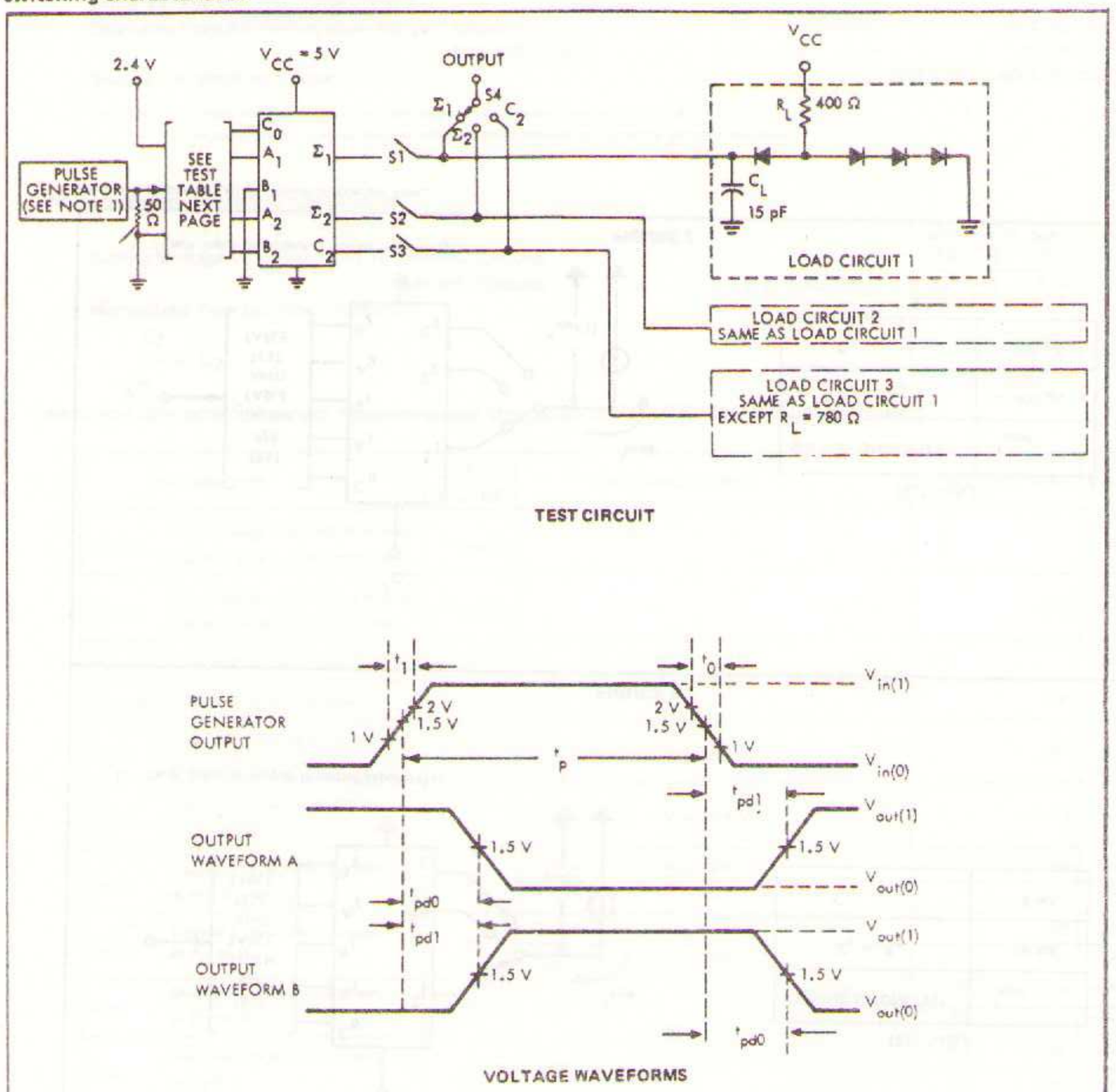
1. Each output is tested separately.

FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES:
1. The generator has the following characteristics: $V_{in(1)} \geq 2.4$ V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table.
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 5—SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

SWITCHING TIMES TEST TABLE (SEE NOTE 7)

TEST NO.	PARAMETER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S4)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	A_2, B_1, B_2	CLOSED	OPEN	OPEN
2	t_{pd0}							
3	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2 and C_0	OPEN	CLOSED	OPEN
4	t_{pd0}							
5	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1, A_2	B_1, B_2	OPEN	CLOSED	CLOSED
6	t_{pd0}							
7	t_{pd1}	C_0	C_2 (WAVEFORM B)	A_1, A_2	B_1, B_2	OPEN	OPEN	CLOSED
8	t_{pd0}							

NOTE 7: Inputs and outputs not otherwise specified are open.

HIGH-SPEED TTL 4-BIT FULL ADDERS FOR APPLICATION IN

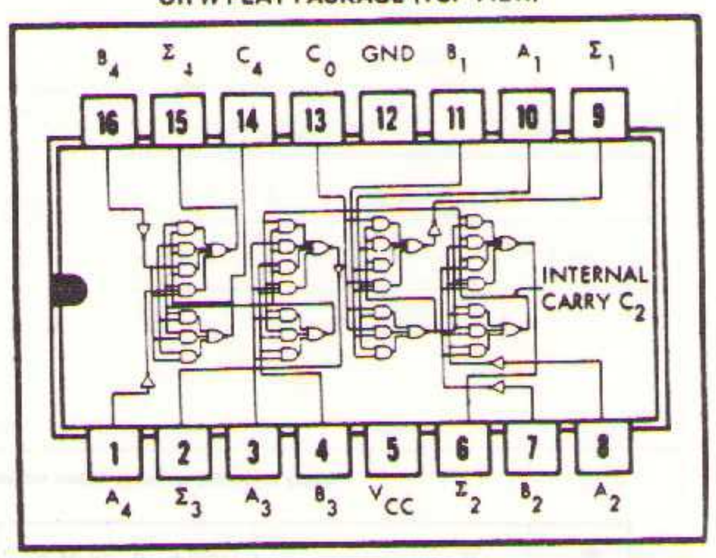
- Digital Computer Systems
- Data-Handling Systems
- Control Systems

logic

INPUT				OUTPUT					
				WHEN $C_0 = 0$ / WHEN $C_2 = 0$			WHEN $C_0 = 1$ / WHEN $C_2 = 1$		
A_1 / A_3	B_1 / B_3	A_2 / A_4	B_2 / B_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4	Σ_1 / Σ_3	Σ_2 / Σ_4	C_2 / C_4
0	0	0	0	0	0	0	1	0	0
1	0	0	0	1	0	0	0	1	0
0	1	0	0	1	0	0	0	1	0
1	1	0	0	0	1	0	1	1	0
0	0	1	0	0	1	0	1	1	0
1	0	1	0	1	1	0	0	0	1
0	1	1	0	1	1	0	0	0	1
1	1	1	0	0	0	1	1	0	1
0	0	0	1	0	1	0	1	1	0
1	0	0	1	1	1	0	0	0	1
0	1	0	1	1	1	0	0	0	1
1	1	0	1	0	0	1	1	0	1
0	0	1	1	0	0	1	1	0	1
1	0	1	1	1	0	1	0	1	1
0	1	1	1	1	0	1	0	1	1
1	1	1	1	0	1	1	1	1	1

NOTE 1: Input conditions at A_1, A_2, B_1, B_2, and C_0 are used to determine outputs Σ_1 and Σ_2, and the value of the internal carry C_2. The values at C_2, A_3, B_3, A_4, and B_4, are then used to determine outputs Σ_3, Σ_4, and C_4.

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

This full adder performs the addition of two 4-bit binary numbers. The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bit. Designed for medium-to-high-speed, multiple-bit, parallel-add/serial-carry applications, the circuit utilizes high-speed, high-fan-out transistor-transistor logic (TTL) but is compatible with both DTL and TTL families. The implementation of a single-inversion, high-speed, Darlington-connected serial-carry circuit within each bit minimizes the necessity for extensive "look-ahead" and carry-cascading circuits. The power dissipation level has been maintained considerably below that attainable with equivalent standard integrated circuits connected to perform four-bit full-adder functions.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5483 Circuits	−55°C to 125°C
	SN7483 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC}: (See Note 1)	SN5483 Circuits	4.5	5	5.5	V
	SN7483 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Outputs:					
C_4				5	
Σ_1, Σ_2, Σ_3 or Σ_4				10	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 2			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1 and 2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	2			2.4			V
$V_{out(0)}$	Logical 0 output voltage	1					0.4	V
$I_{in(0)}$	Logical 0 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 0.4 V			−6.4	mA
$I_{in(0)}$	Logical 0 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
$I_{in(1)}$	Logical 1 level input current at A_1, A_3, B_1, B_3, or C_0	3	V_{CC} = MAX,	V_{in} = 2.4 V			160	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at A_2, A_4, B_2, or B_4	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current at Σ_1, Σ_2, Σ_3, or Σ_4§	4	V_{CC} = MAX	SN 5483	−20		−55	mA
				SN7483	−18		−55	mA
I_{OS}	Short-circuit output current at C_4§	4	V_{CC} = MAX	SN5483	−20		−70	mA
				SN7483	−18		−70	mA
I_{CC}	Supply Current	3	V_{CC} = MAX,	SN5483		78	110	mA
				SN7483		78	128	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

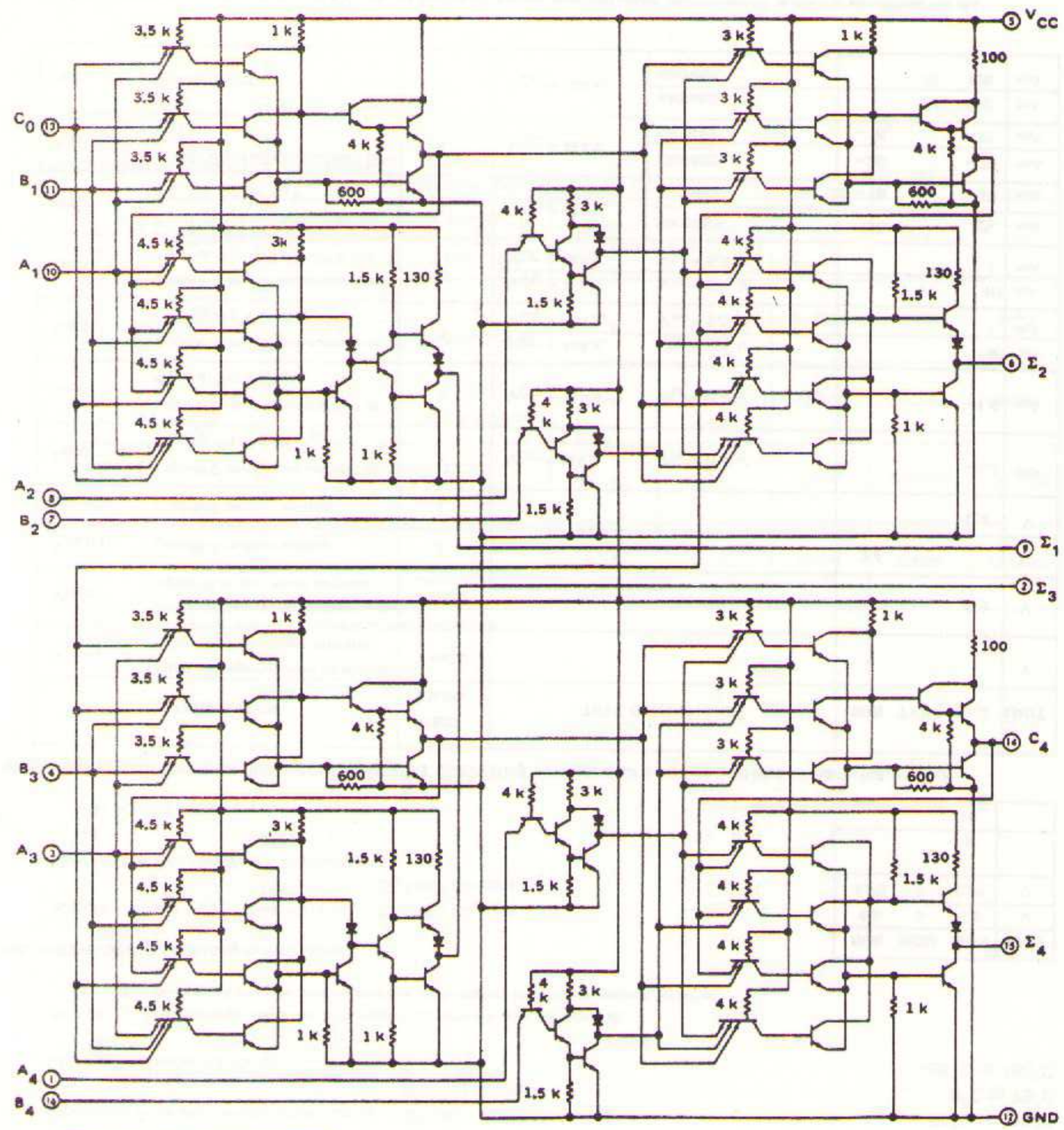
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (unless otherwise noted N = 10)

PARAMETER§	FROM (INPUT)	TO (OUTPUT)	FIGURE 5 TEST NO.	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	C_0	1	1	C_L = 15 pF, R_L = 400 Ω			34	ns
t_{pd0}			2	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd1}	C_0	2	3	C_L = 15 pF, R_L = 400 Ω			38	ns
t_{pd0}			4	C_L = 15 pF, R_L = 400 Ω			42	ns
t_{pd1}	C_0	3	5	C_L = 15 pF, R_L = 400 Ω			50	ns
t_{pd0}			6	C_L = 15 pF, R_L = 400 Ω			60	ns
t_{pd1}	C_0	4	7	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd0}			8	C_L = 15 pF, R_L = 400 Ω			55	ns
t_{pd1}	C_0	C_4	9	C_L = 15 pF, R_L = 780 Ω		35	48	ns
t_{pd0}			10	C_L = 15 pF, R_L = 780 Ω		22	32	ns
t_{pd1}	A_2 or B_2	2	11 and 13	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			12 and 14	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd1}	A_4 or B_4	4	15 and 17	C_L = 15 pF, R_L = 400 Ω			40	ns
t_{pd0}			16 and 13	C_L = 15 pF, R_L = 400 Ω			35	ns

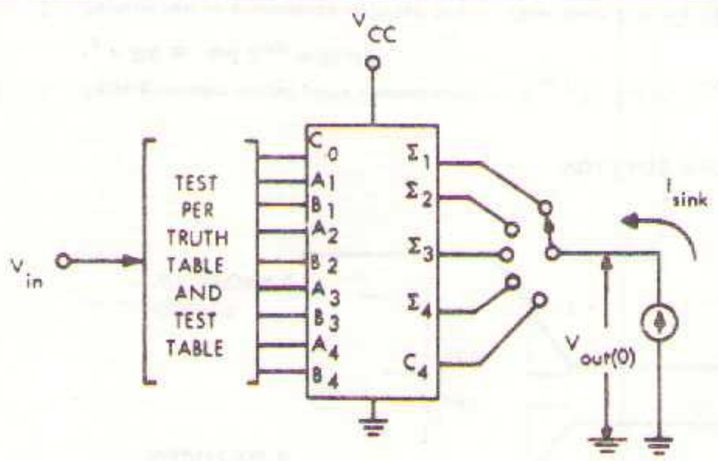
§ t_{pd1} is propagation delay time to logical 1 level. t_{pd0} is propagation delay time to logical 0 level.

schematic



Component values shown are nominal.
Resistor values are in ohms.

d-c test circuits†

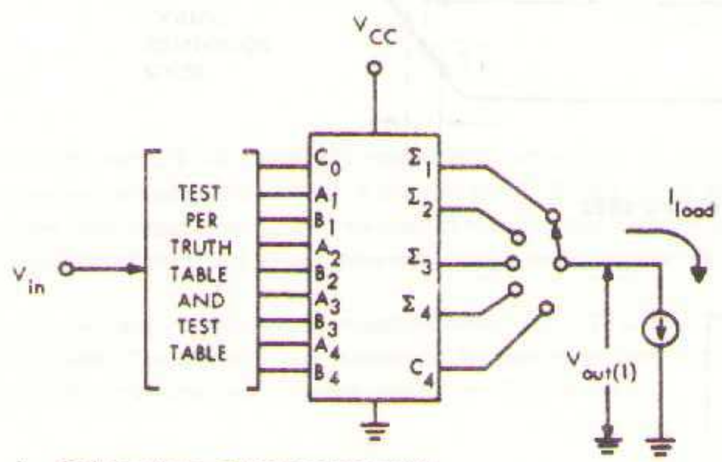


TEST TABLE

OUTPUT UNDER TEST	I_{sink}
Σ_1, Σ_2, Σ_3, or Σ_4	16 mA
C_4	8 mA

1. Each input or output is tested separately.

FIGURE 1



TEST TABLE

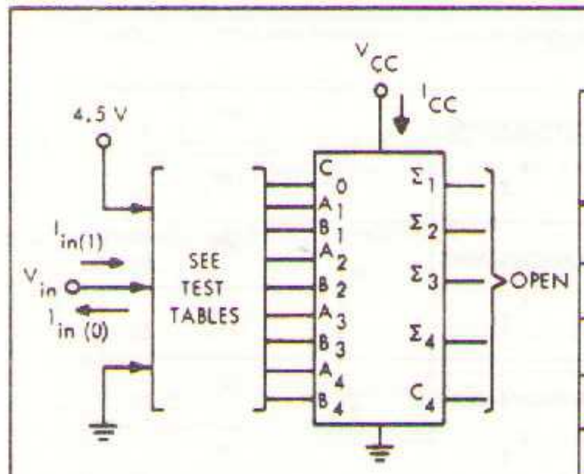
OUTPUT UNDER TEST	I_{load}
Σ_1, Σ_2, Σ_3, or Σ_4	− 400 μA
C_4	− 200 μA

1. Each input or output is tested separately.

FIGURE 2

†Arrows indicate actual direction of current flow.

d-c test circuits† (continued)



1. Each input is tested separately.
2. When testing I_{CC} apply 4.5 V to A_1, A_2, A_3, A_4, and C_0; and ground B_1, B_2, B_3 and B_4.

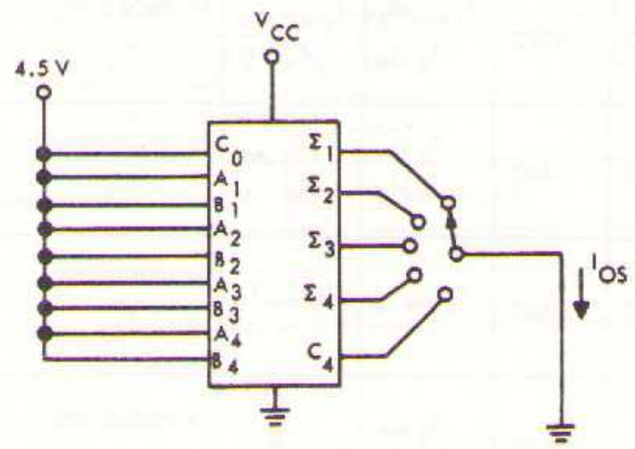
$I_{in(0)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	APPLY 4.5 V
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

$I_{in(1)}$ TEST TABLE

APPLY V_{in} TEST I_{in}	GND
C_0	A_1 and B_1
A_1	C_0 and B_1
B_1	C_0 and A_1
A_2	None
B_2	None
A_3	A_2, B_2, and B_3
B_3	A_2, B_2, and A_3
A_4	None
B_4	None

FIGURE 3



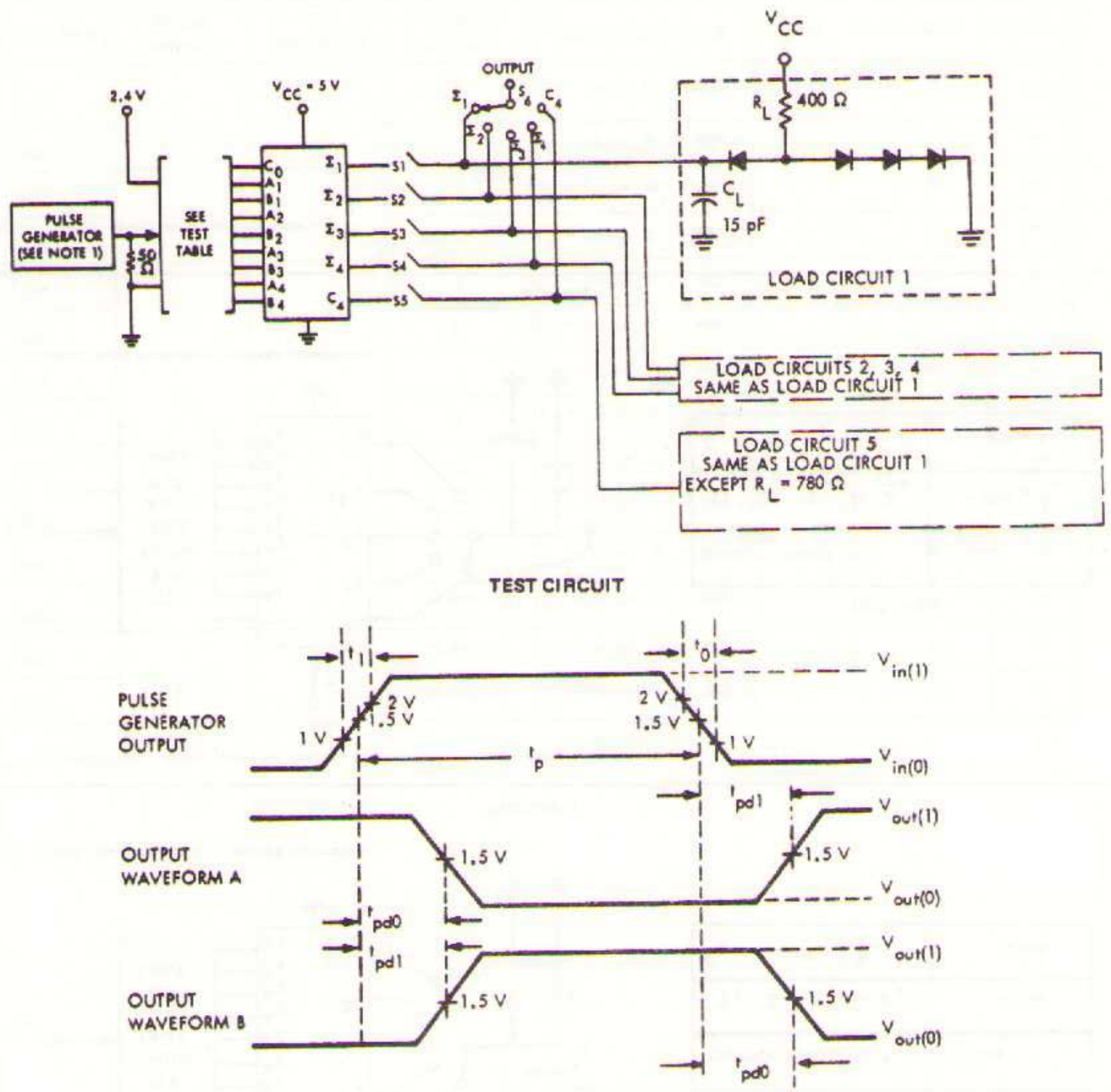
1. Each output is tested separately.

FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTES:
1. Pulse generator output pulse characteristics: $V_{in(1)} \leq 2.4$ V, $V_{in(0)} \leq 0.4$ V, t_1 = 8 to 15 ns, t_0 = 3 to 5 ns, PRR = 1 MHz, t_p = 200 ns, and $Z_{out} \approx 50\ \Omega$.
2. Perform test in accordance with test table. (See sheet 2 of this figure.)
3. Each output is tested separately.
4. Voltage values are with respect to network ground terminal.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064

FIGURE 5—SWITCHING TIMES (SHEET 1 OF 2)

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

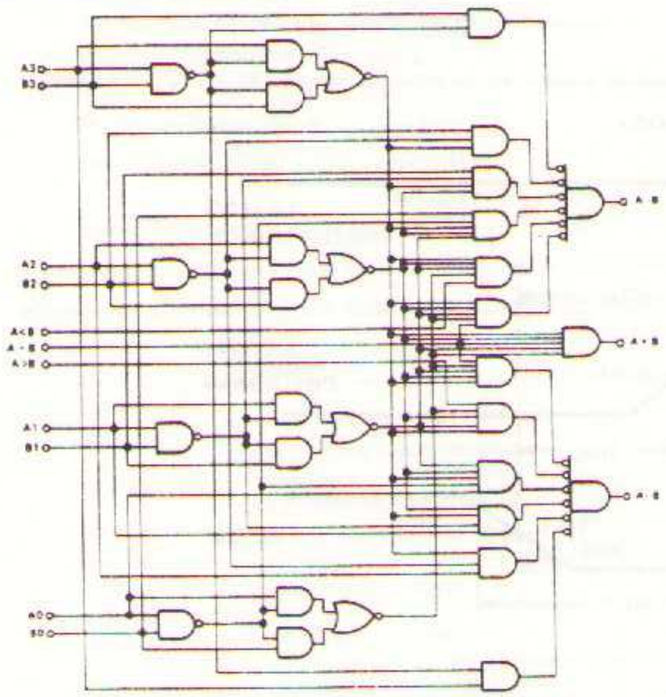
TEST TABLE (SEE NOTE 7)

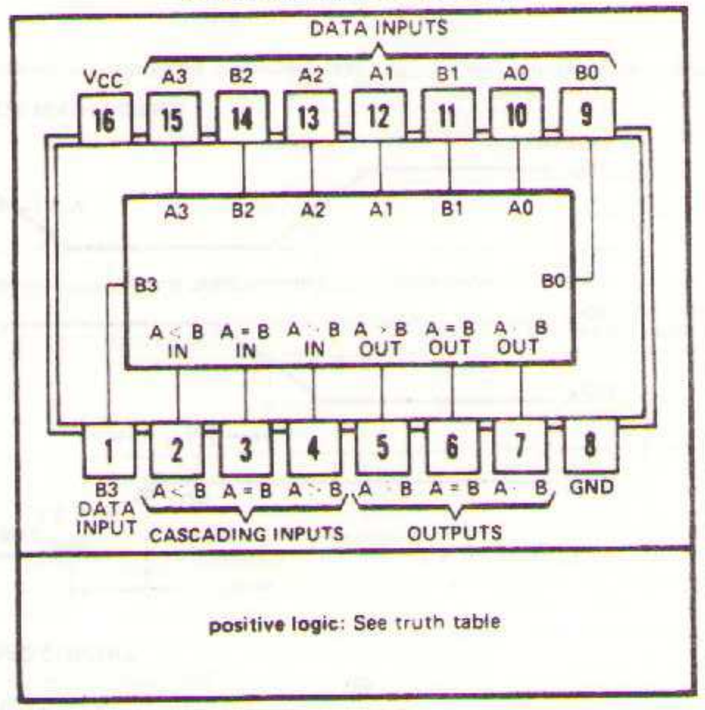
TEST NO.	PARA-METER	APPLY PULSE GENERATOR OUTPUT TO	OUTPUT UNDER TEST (S6)	APPLY 2.4 V TO	APPLY GND TO	S1	S2	S3	S4	S5
1	t_{pd1}	C_0	Σ_1 (WAVEFORM A)	A_1	B_1, A_2, and B_2	CLOSED	OPEN	OPEN	OPEN	OPEN
2	t_{pd0}									
3	t_{pd1}	C_0	Σ_2 (WAVEFORM A)	A_1 and A_2	B_1 and B_2	OPEN	CLOSED	OPEN	OPEN	OPEN
4	t_{pd0}									
5	t_{pd1}	C_0	Σ_3 (WAVEFORM A)	A_1, A_2, and A_3	B_1, B_2, and B_3	OPEN	OPEN	CLOSED	OPEN	OPEN
6	t_{pd0}									
7	t_{pd1}	C_0	Σ_4 (WAVEFORM A)	A_1, A_2, A_3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	CLOSED
8	t_{pd0}									
9	t_{pd1}	C_0	C_4 (WAVEFORM B)	A_1, A_2, A3, and A_4	B_1, B_2, B_3, and B_4	OPEN	OPEN	OPEN	OPEN	CLOSED
10	t_{pd0}									
11	t_{pd1}	A_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, B_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
12	t_{pd0}									
13	t_{pd1}	B_2	Σ_2 (WAVEFORM B)	None	A_1, B_1, A_2, and C_0	OPEN	CLOSED	OPEN	OPEN	OPEN
14	t_{pd0}									
15	t_{pd1}	A_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and B_4	OPEN	OPEN	OPEN	CLOSED	OPEN
16	t_{pd0}									
17	t_{pd1}	B_4	Σ_4 (WAVEFORM B)	None	A_3, B_3, and A_4	OPEN	OPEN	OPEN	CLOSED	OPEN
18	t_{pd0}									

NOTE 7: Inputs and outputs not otherwise specified are open.

FIGURE 5 – SWITCHING TIMES (SHEET 2 of 2)

functional block diagram





†Pin assignments for these circuits are the same for all packages.

description

The SN5485 and SN7485 perform magnitude comparison of straight binary and straight BCD (8421) codes. Three fully decoded decisions about two 4-bit words (A, B) are made and are externally available at three outputs. These devices are fully expandable to any number of bits without external gates. When cascaded, the total time for comparison is the function of the word length; however, only a two-gate-level delay (12 ns) is added for each four-bit expansion.

These circuits are completely compatible with most TTL and DTL families. Typical average power dissipation is 275 milliwatts. The SN5485 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN7485 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A > B	A < B	A = B	A > B	A < B	A = B
A3 > B3	X	X	X	X	X	X	H	L	L
A3 < B3	X	X	X	X	X	X	L	H	L
A3 = B3	A2 > B2	X	X	X	X	X	H	L	L
A3 = B3	A2 < B2	X	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 > B1	X	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 < B1	X	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 > B0	X	X	X	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 < B0	X	X	X	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	H	L	L	H	L	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	H	L	L	H	L
A3 = B3	A2 = B2	A1 = B1	A0 = B0	L	L	H	L	L	H

NOTE: H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN5485 Circuits	−55°C to 125°C
SN7485 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	SN5485			SN7485			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†			MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage					2			V
V_{IL} Low-level input voltage							0.8	V
V_I Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA				−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA		2.4			V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA				0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V				1	mA
I_{IH} High-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 2.4 V				40	μA
	all other inputs						120	
I_{IL} Low-level input current	A < B, A > B inputs	V_{CC} = MAX,	V_I = 0.4 V				−1.6	mA
	all other inputs						−4.8	
I_{OS} Short-circuit output current§		V_{CC} = MAX,	V_O = 0	SN5485	−20		−55	mA
				SN7485	−18		−55	
I_{CC} Supply current		V_{CC} = MAX,	See Note 3			55	88	mA

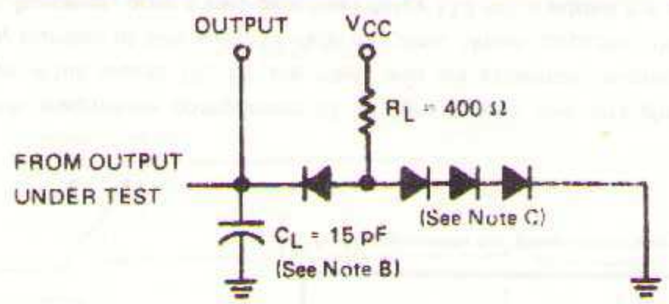
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.
NOTE 3: I_{CC} is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

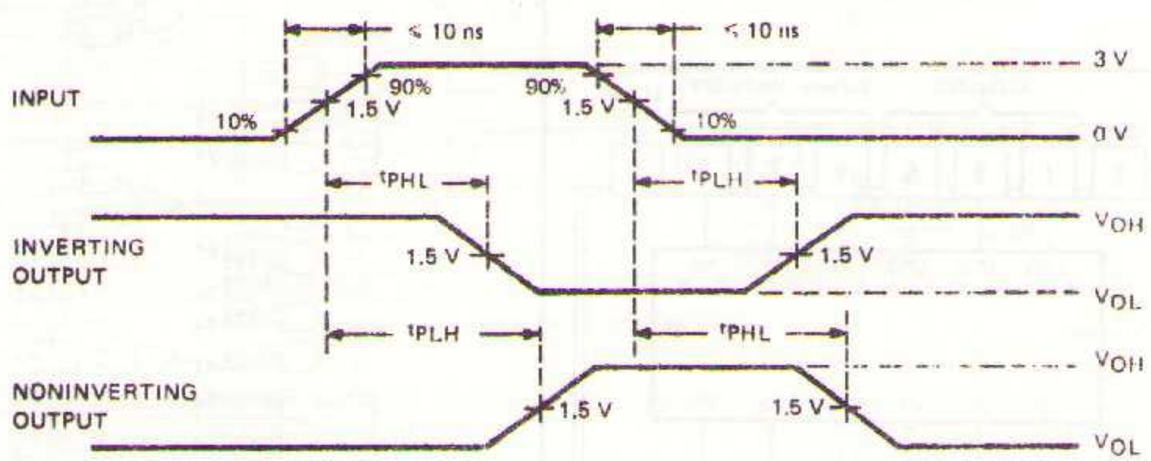
PARAMETER¶	FROM INPUT	TO OUTPUT	NUMBER OF GATE LEVELS	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any A or B data input	A < B, A > B	1	C_L = 15 pF, R_L = 400 Ω, See Figure 1		7		ns
			2			12		
			3			17	26	
		A = B	4			23	35	
t_{PHL}	Any A or B data input	A < B, A > B	1			11		ns
			2			16		
			3			20	30	
		A = B	4			20	30	
t_{PLH}	A < B or A = B	A > B	1			7	11	ns
t_{PHL}	A < B or A = B	A > B	1			11	17	ns
t_{PLH}	A = B	A = B	2			13	20	ns
t_{PHL}	A = B	A = B	2			11	17	ns
t_{PLH}	A > B or A = B	A < B	1			7	11	ns
t_{PHL}	A > B or A = B	A < B	1			11	17	ns

¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. Input pulses are supplied by a pulse generator having the following characteristics: PRR ≤ 1 MHz, duty cycle ≈ 50%, Z_{out} ≈ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

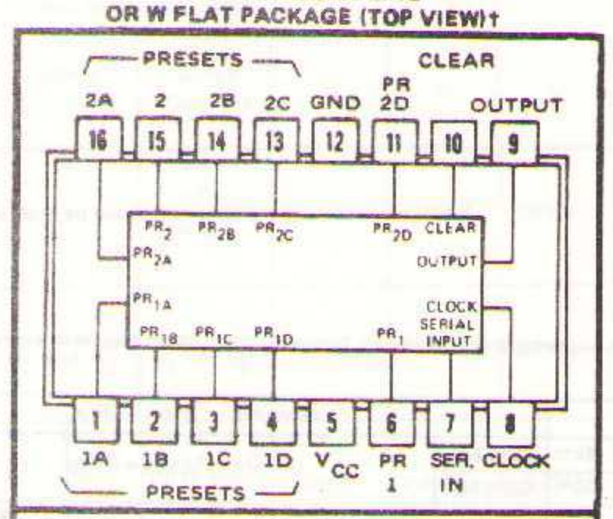
FIGURE 1--PROPAGATION DELAY TIMES

TTL MSI PARALLEL-IN SERIAL-OUT REGISTERS

for application as

- Dual-Source, Parallel-To-Serial Converter
- Serial-In Serial-Out Register

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: High input to clear sets Q_A, Q_B, Q_C, and Q_D to logical 0.

†Pin assignments for these circuits are the same for all packages.

description

This monolithic shift register, utilizing transistor-transistor logic (TTL) circuits in the familiar Series 74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, and four inverter-drivers. Internal interconnections of these functions provide a versatile register which performs right-shift operations as a serial-in, serial-out register or as a dual-source, parallel-to-serial converter. A number of these registers may be connected in series to form an n-bit register.

All flip-flops are simultaneously set to the logical 0 state by applying a logical 1 voltage to the clear input. This condition may be applied independent of the state of the clock input, but not independent of state of the preset input. Preset input is independent of the clock and clear states.

The flip-flops are simultaneously set to the logical 1 state from either of two preset input sources. Preset inputs 1A through 1D are activated during the time that a positive pulse is applied to preset 1 if preset 2 is at a logical 0 level. When the logic levels at preset 1 and preset 2 are reversed, preset inputs 2A through 2D are active.

Transfer of information to the outputs occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information for the first flip-flop. The outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input, preset 1, and preset 2 must be at a logical 0 when clocking occurs.

This register is completely compatible for use with TTL and DTL logic circuits and when used with other TTL circuits, noise margins are typically one volt. Typical average power dissipation is 175 milliwatts, and propagation delay times from clock to output are typically 25 nanoseconds.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5494 Circuits	−55°C to 125°C
	SN7494 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. The voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5494 Circuits	4.5	5	5.5	V
SN7494 Circuits	4.75	5	5.25	V
Normalized Fan-Out From Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time: $t_{setup(1)}$	35			ns
$t_{setup(0)}$	25			ns
Serial Input Hold Time, t_{hold}	0			

NOTE: 1. These voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

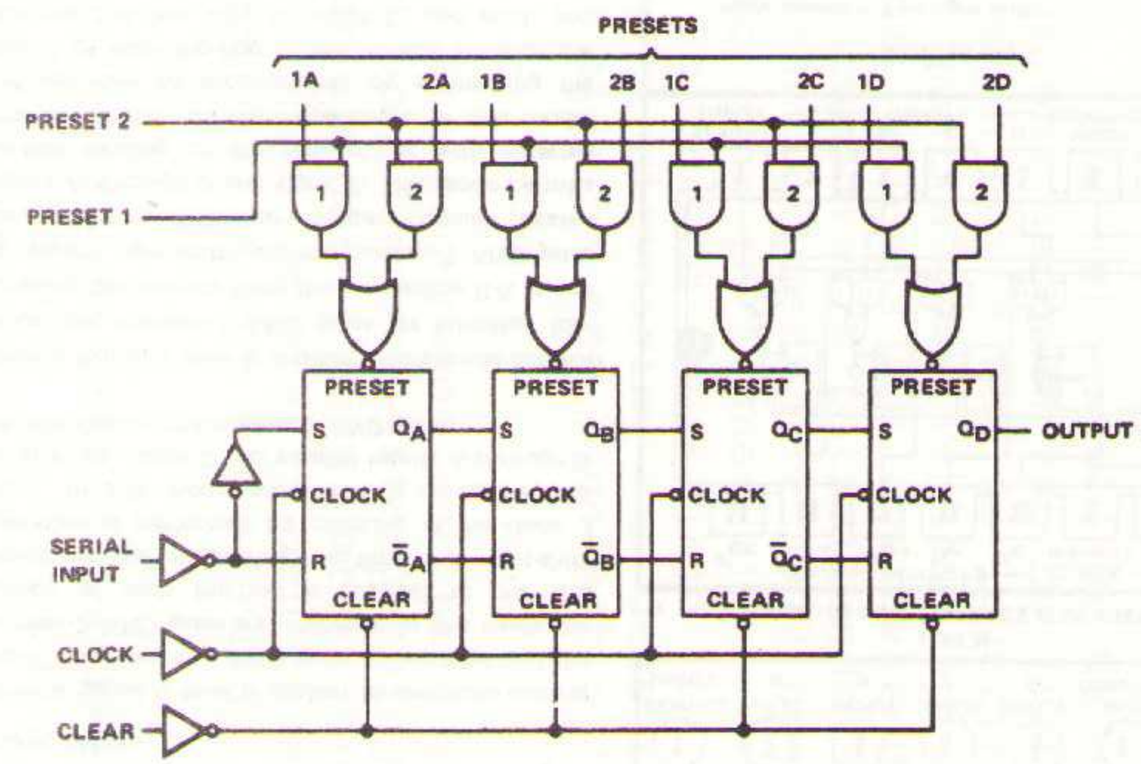
PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal					0.8	V
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 2.4 V				160	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset 1 and preset 2	V_{CC} = MAX, V_{in} = 0.4 V				−6.4	mA
I_{OS}	Short-circuit input current§	V_{CC} = MAX, V_{out} = 0	SN5494	−20		−57	mA
			SN7494	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5494		35	50	mA
			SN7494		35	58	mA

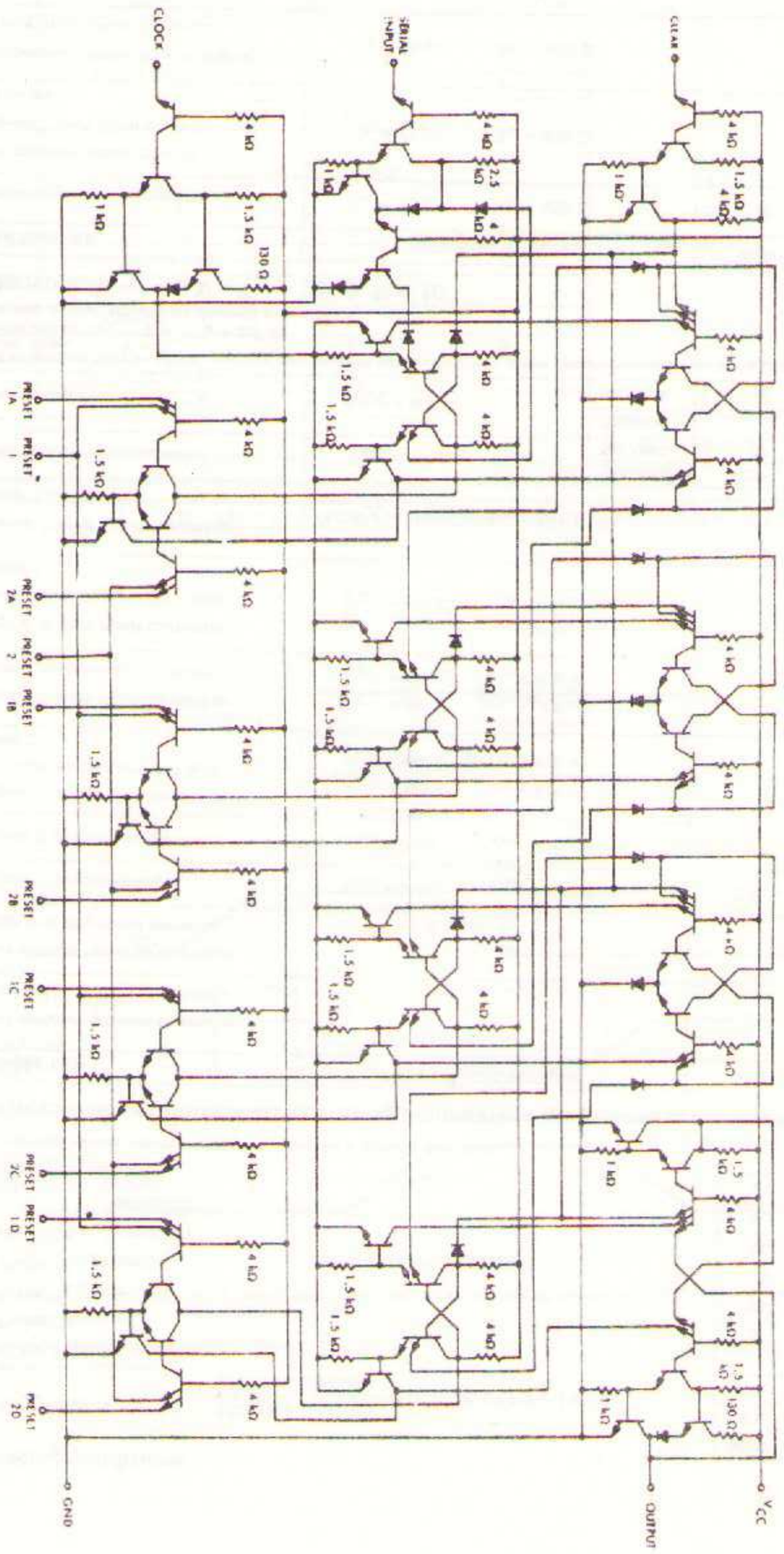
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset to output	C_L = 15 pF, R_L = 400 Ω			35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			40	ns

functional block diagram





Component values shown are nominal.

A TTL MSI PARALLEL-IN PARALLEL-OUT REGISTER

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Registe

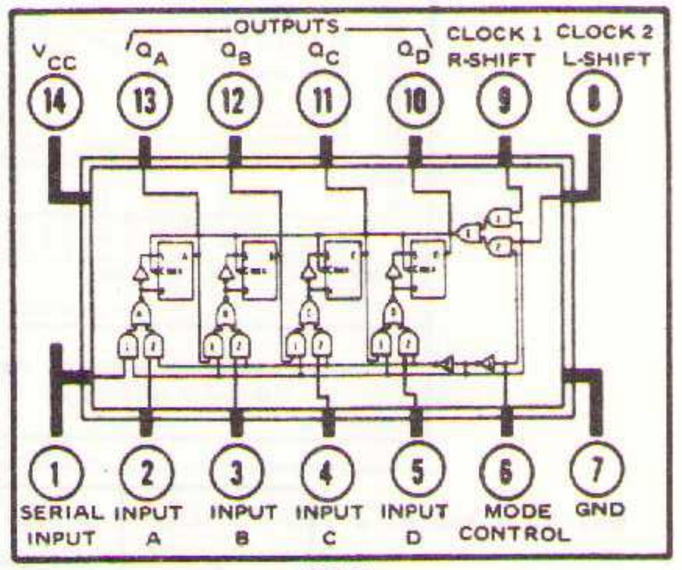
description

This monolithic shift register, utilizing transistor-transistor-logic (TTL) circuits in the familiar Series 54/74 configuration, is composed of four R-S master-slave flip-flops, four AND-OR-INVERT gates, one AND-OR gate, and six inverters-drivers. Internal interconnections of these functions provide a versatile register which will perform right-shift or left-shift operations dependent upon the logical input level to the mode control. A number of these registers may be connected in series to form an n-bit right-shift or left-shift register. This register can also be used as a parallel-in, parallel-out storage register with gate (mode) control.

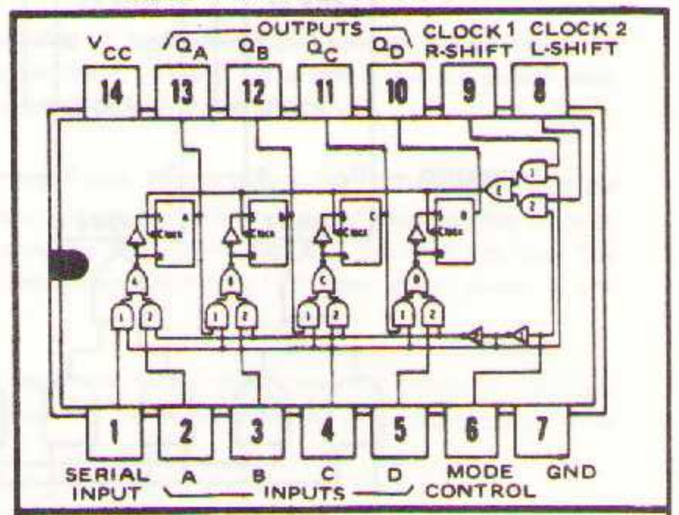
When a logical 0 level is applied to the mode control input, the number-1 AND gates are enabled and the number-2 AND gates are inhibited. In this mode the output of each flip-flop is coupled to the R-S inputs of the succeeding flip-flop and right-shift operation is performed by clocking at the clock 1 input. In this mode, serial data is entered at the serial input. Clock 2 and parallel inputs A through D are inhibited by the number-2 AND gates.

When a logical 1 level is applied to the mode control input, the number-1 AND gates are inhibited (decoupling the outputs from the succeeding R-S inputs to prevent right-shift) and the number-2 AND gates are enabled to allow entry of data through parallel inputs A through D and clock 2. This mode permits parallel loading of the register, or with external interconnection, shift-left operation. In this mode, shift-left can be accomplished by connecting the output of each flip-flop to the parallel input of the previous flip-flop (Q_D to input C, and etc.), and serial data is entered at input D.

W
FLAT PACKAGE (TOP VIEW)



J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic

Mode control = 0 for right shift
Mode control = 1 for left shift or parallel load

Clocking for the shift register is accomplished through the AND-OR gate E which permits separate clock sources to be used for the shift-right and shift-left modes. If both modes can be clocked from the same source, the clock input may be applied commonly to clock 1 and clock 2. Information must be present at the R-S inputs of the master-slave flip-flops prior to clocking. Transfer of information to the output pins occurs when the clock input goes from a logical 1 to a logical 0.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Average power dissipation is typically 195 milliwatts. The SN5495A and SN7495A are unilaterally interchangeable with and replace SN5495 and SN7495, respectively, but offer diode-clamped inputs, improved speed, and reduced power dissipation.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5495A Circuits	−55°C to 125°C
	SN7495A Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN5495A Circuits	4.5	5	5.5	V
	SN7495A Circuits	4.75	5	5.25	V
Normalized Fan-Out From Each Output:	High logic level			20	
	Low logic level			10	
Width of Clock Pulse $t_{p(clock)}$ (See Figure 9):	SN5495A Circuits	20	10		ns
	SN7495A Circuits	15	10		ns
Setup Time Required at Serial, A, B, C, or D Inputs t_{setup} (See Figure 9)		10			ns
Hold Time Required at Serial, A, B, C, or D Inputs t_{hold} (See Figure 9)		0			ns
Logical 0 Level Setup Time Required at Mode Control (t1 in Figure 10) (With Respect to Clock 1 input)		15			ns
Logical 1 Level Setup Time Required at Mode Control (t2 in Figure 10) (With Respect to Clock 2 input)		15			ns
Logical 0 Level Setup Time Required at Mode Control (t3 in Figure 10) (With Respect to Clock 2 input)		5			ns
Logical 1 Level Setup Time Required at Mode Control (t4 in Figure 10) (With Respect to Clock 1 input)		5			ns

NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltages must be zero or positive with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1 and 3		2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2 and 4				0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 and 3	V_{CC} = MIN, I_{load} = −800 μA	2.4			V
$V_{out(0)}$	Logical 0 output voltage	2 and 4	V_{CC} = MIN, I_{sink} = 16 mA			0.4	V
$I_{in(0)}$	Logical 0 level input current at any input except mode control	5	V_{CC} = MAX, V_{in} = 0.4 V			−1.6	mA
$I_{in(0)}$	Logical 0 level input current at mode control	5	V_{CC} = MAX, V_{in} = 0.4 V			−3.2	mA
$I_{in(1)}$	Logical 1 level input current at any input except mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			40	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
$I_{in(1)}$	Logical 1 level input current at mode control	6	V_{CC} = MAX, V_{in} = 2.4 V			80	μA
			V_{CC} = MAX, V_{in} = 5.5 V			1	mA
I_{OS}	Short-circuit output current§	7	V_{CC} = MAX	−18		−57	mA
I_{CC}	Supply current	8	V_{CC} = MAX	39		63	mA

† For conditions shown as MIN or MAX use the appropriate value specified under recommended operating conditions for the particular circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

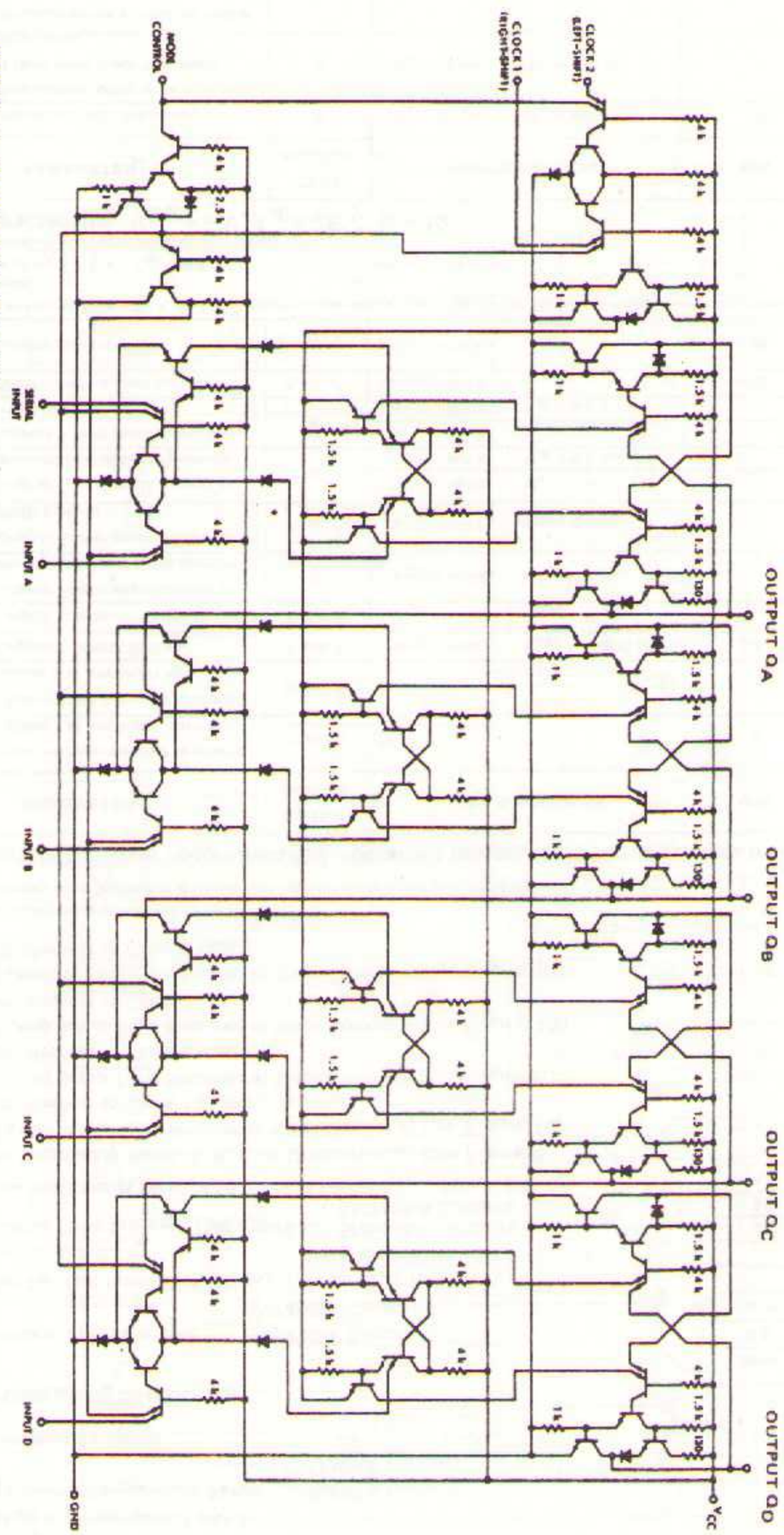
PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP	MAX	UNIT
f_{max}	Maximum shift frequency	9	C_L = 15 pF, R_L = 400 Ω	25	36		MHz
t_{pd1}	Propagation delay time to logical 1 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		18	27	ns
t_{pd0}	Propagation delay time to logical 0 level from clock 1 or clock 2 to outputs	9	C_L = 15 pF, R_L = 400 Ω		21	32	ns

OPELEC VERTEGENWOORDIGING

Sinds januari 1972 hebben wij de Nederlandse alleenvertegenwoordiging op ons genomen van de Franse firma Opelec. Deze firma houdt zich bezig met de levering van een groot assortiment instrumentkasten, rekken, apparatenkoffers, insteeksystemen, enz. volgens het overbekende 19" systeem. Een informatieve documentatie betreffende dit programma wordt in onze Technische Documentatie 1972 opgenomen. Om echter op zijn best de uitvoering te kunnen zien, adviseren wij U eens in onze showroom te Rotterdam een kijkje te nemen. U zult dan zien, dat de afwerking en uitvoering van deze kastensystemen alleen al concurrerend zijn en een regelmatig 'Opelec'-gebruiker gaan worden.

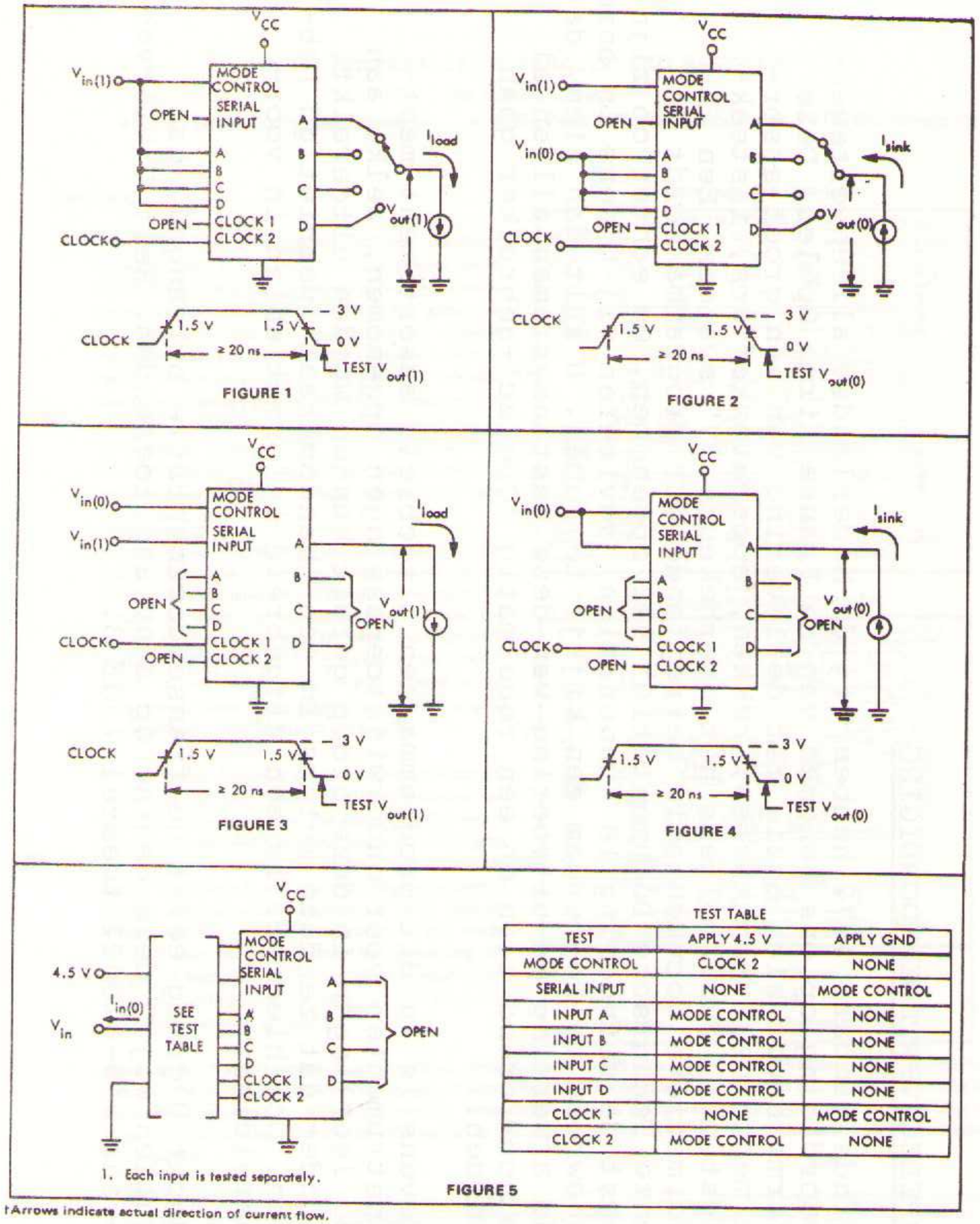
Tevens is in dit programma een uitgebreid assortiment meetinstrumenten voor onderwijstoepassingen opgenomen, welke aan de leerlingen in deze groep gerust kunnen worden uitgereikt, zonder dat ze deze meters in een 'handomdraai' vernietigd hebben. Ook hierover is een uitgebreid informatieblad in voorbereiding.

Mocht U graag eerst de franse documentatie ontvangen, dan zullen wij U deze gaarne op aanvraag toezenden. Belt U hiervoor even: 010-670022 toestel 7 of 3.



NOTES: 1. Resistor values are in ohms.
2. Component values shown are nominal.

d-c test circuits†

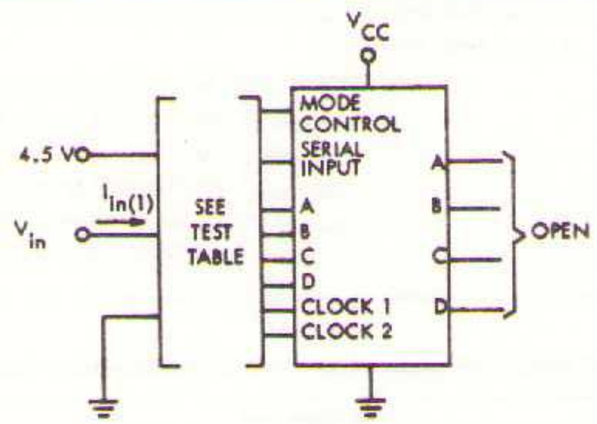


TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	CLOCK 2	NONE
SERIAL INPUT	NONE	MODE CONTROL
INPUT A	MODE CONTROL	NONE
INPUT B	MODE CONTROL	NONE
INPUT C	MODE CONTROL	NONE
INPUT D	MODE CONTROL	NONE
CLOCK 1	NONE	MODE CONTROL
CLOCK 2	MODE CONTROL	NONE

†Arrows indicate actual direction of current flow.

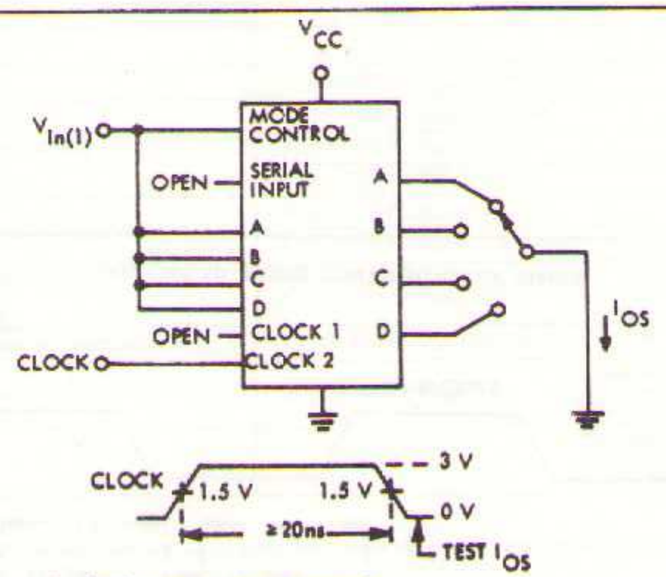
d-c test circuits† (continued)



TEST TABLE

TEST	APPLY 4.5 V	APPLY GND
MODE CONTROL	NONE	CLOCK 2
SERIAL INPUT	MODE CONTROL	NONE
INPUT A	NONE	MODE CONTROL
INPUT B	NONE	MODE CONTROL
INPUT C	NONE	MODE CONTROL
INPUT D	NONE	MODE CONTROL
CLOCK 1	MODE CONTROL	NONE
CLOCK 2	NONE	MODE CONTROL

FIGURE 6



1. Each output is tested separately.

FIGURE 7

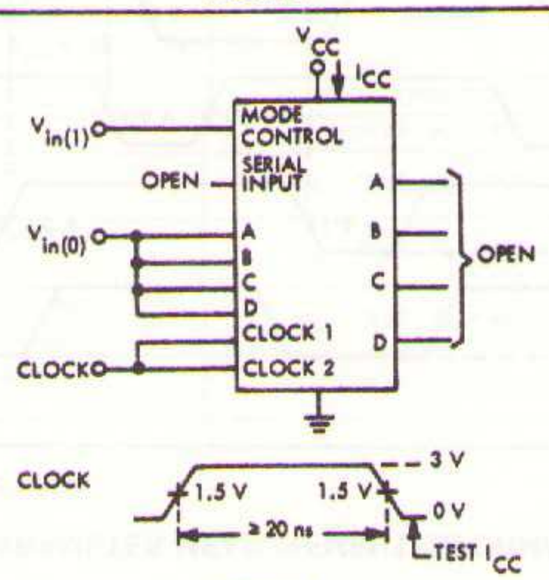
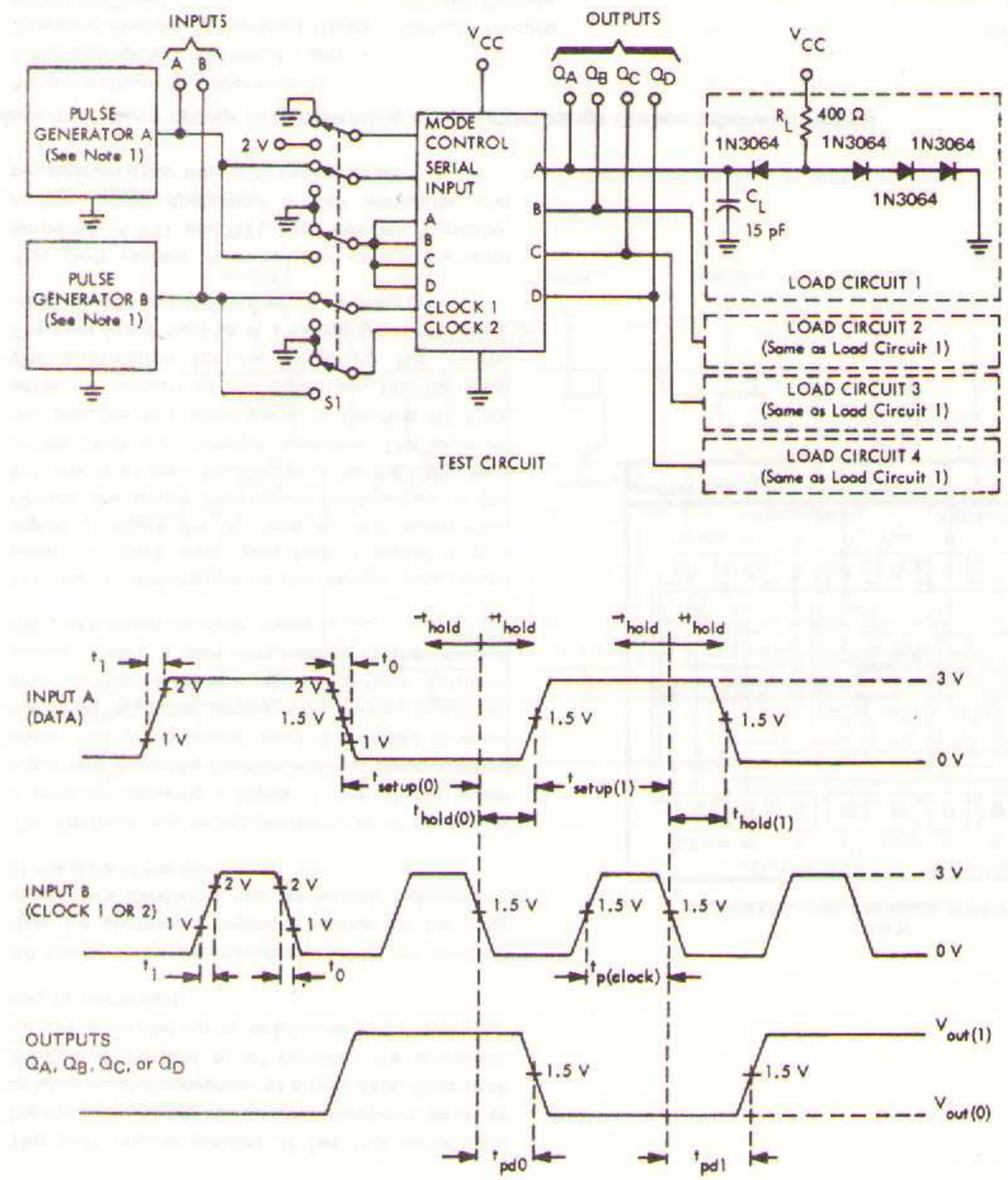


FIGURE 8

† Arrows indicate actual direction of current flow.

switching charateristics



VOLTAGE WAVEFORMS

NOTES: 1. The pulse generators have the following characteristics: V_{gen} = 3 V, $t_1 = t_0 \leq$ 10 ns, and $Z_{out} \approx$ 50 Ω. For pulse generator A : $t_p \geq$ 20 ns and PRR = 500 kHz. For pulse generator B : $t_p \geq$ 15 ns and PRR = 1 MHz. When testing f_{max} vary PRR.

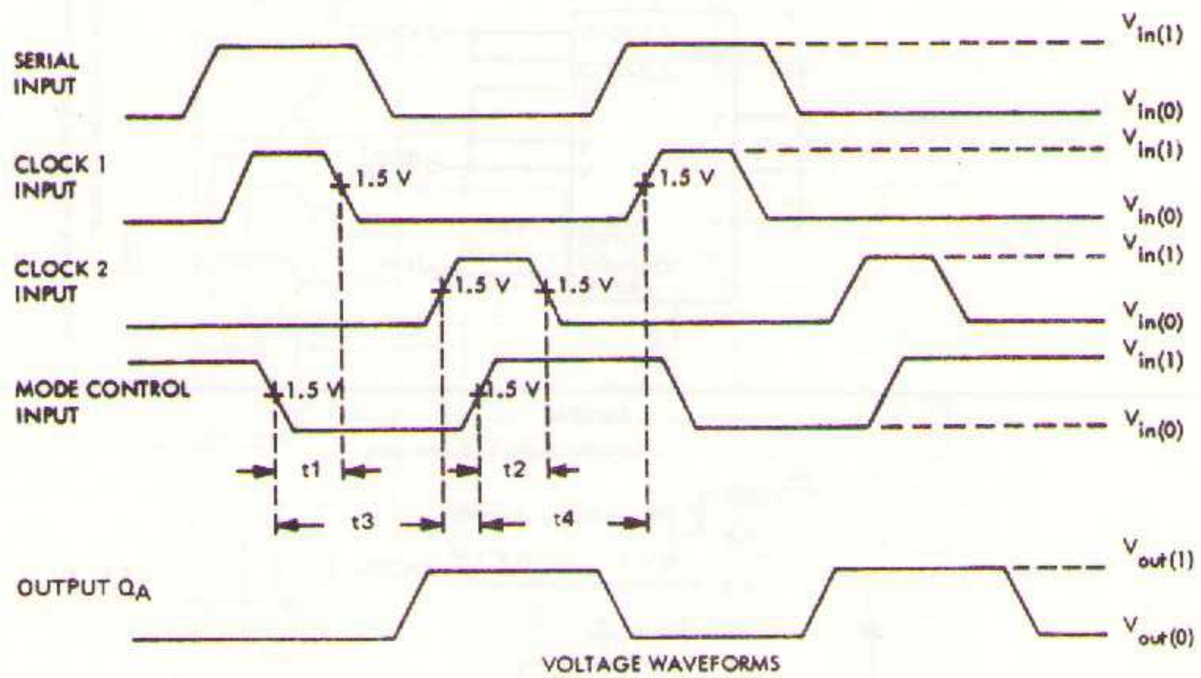
2. Voltage values are with respect to network ground terminal.

3. C_L includes probe and jig capacitance.

FIGURE 9—SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION

recommended mode control setup times



NOTE: Input A is at $V_{in(0)}$.

FIGURE 10—MODE CONTROL SETUP TIMES

TTL MSI MULTIFUNCTION SHIFT REGISTERS

for application as

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

description

This shift register consists of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs to all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

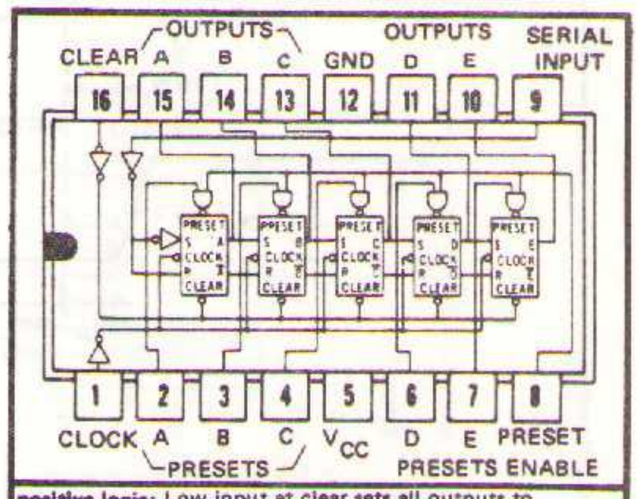
All flip-flops are simultaneously set to the logical 0 state by applying a logical 0 voltage to the clear input. This condition may be applied independent of the state of the clock input.

The flip-flops may be independently set to the logical 1 state by applying a logical 1 to both the preset input of the specific flip-flop and the common preset input. The preset-enable input is provided to allow flexibility of either setting each flip-flop independently or setting two or more flip-flops simultaneously. Preset is also independent of the state of the clock input or clear input.

Transfer of information to the output pins occurs when the clock input goes from a logical 0 to a logical 1. Since the flip-flops are R-S master-slave circuits, the proper information must appear at the R-S inputs of each flip-flop prior to the rising edge of the clock input voltage waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be at a logical 1 and the preset input must be at a logical 0 when clocking occurs.

This shift register is completely compatible with Series 54/74 TTL and DTL logic families. Typically, average power dissipation is 240 milliwatts, and propagation delay time is 25 nanoseconds.

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



positive logic: Low input at clear sets all outputs to logical 0.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Notes 1 and 2)		5.5 V
Operating Free-Air Temperature Range:	SN5496 Circuits	−55°C to 125°C
	SN7496 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTES: 1. These voltage values are with respect to network ground terminal.
2. Input signals must be zero or positive with respect to network ground terminal.

recommended operating conditions

	MIN	TYP	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN5496 Circuits	4.5	5	5.5	V
SN7496 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Output			10	
Width of Clock Pulse, $t_{p(clock)}$	35			ns
Width of Clear Pulse, $t_{p(clear)}$	30			ns
Width of Preset Pulse, $t_{p(preset)}$	30			ns
Serial Input Setup Time, t_{setup}	30			ns
Serial Input Hold Time, t_{hold}	0			ns

NOTE 1: This voltage value is with respect to network ground terminal.

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Logical 1 input voltage			2			V
$V_{in(0)}$	Logical 0 input voltage					0.8	
$V_{out(1)}$	Logical 1 output voltage	V_{CC} = MIN, I_{load} = −400 μA		2.4	3.5		V
$V_{out(0)}$	Logical 0 output voltage	V_{CC} = MIN, I_{sink} = 16 mA			0.22	0.4	V
$I_{in(1)}$	Logical 1 level input current at any input except preset-enable	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(1)}$	Logical 1 level input current at preset-enable	V_{CC} = MAX, V_{in} = 2.4 V				200	μA
		V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at any input except preset-enable	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(0)}$	Logical 0 level input current at preset-enable	V_{CC} = MAX, V_{in} = 0.4 V				−8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_{out} = 0	SN5496	−20		−57	mA
			SN7496	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX	SN5496		48	68	mA
			SN7496		48	79	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

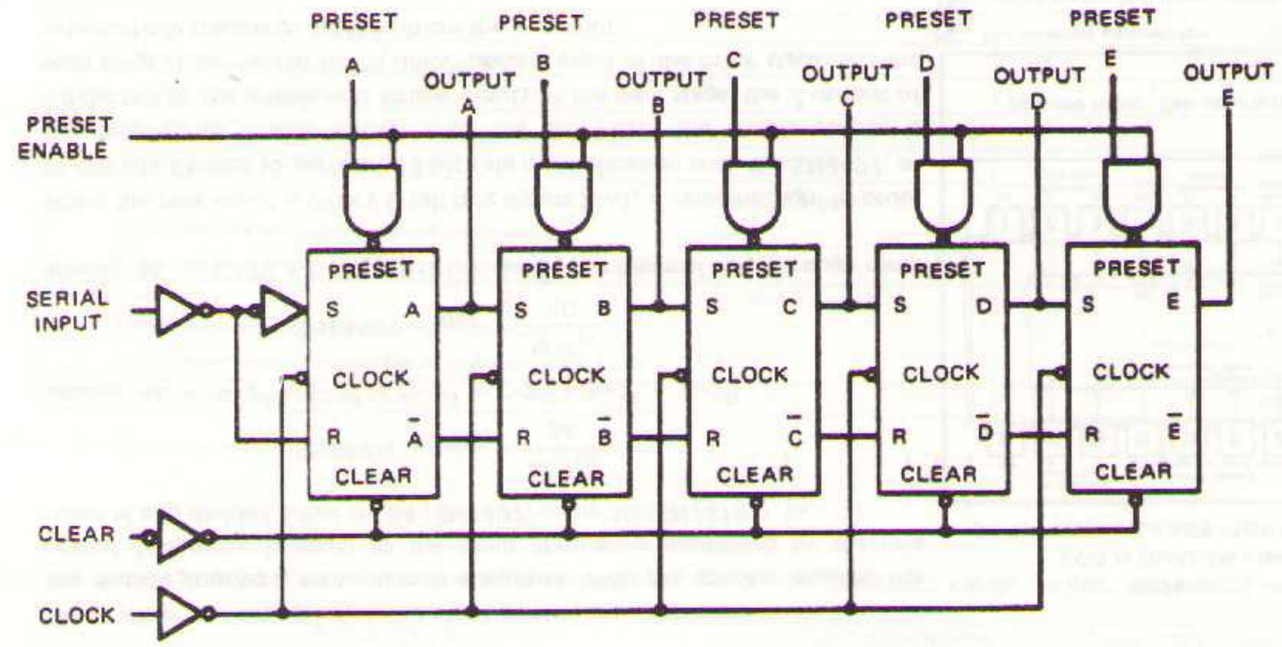
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

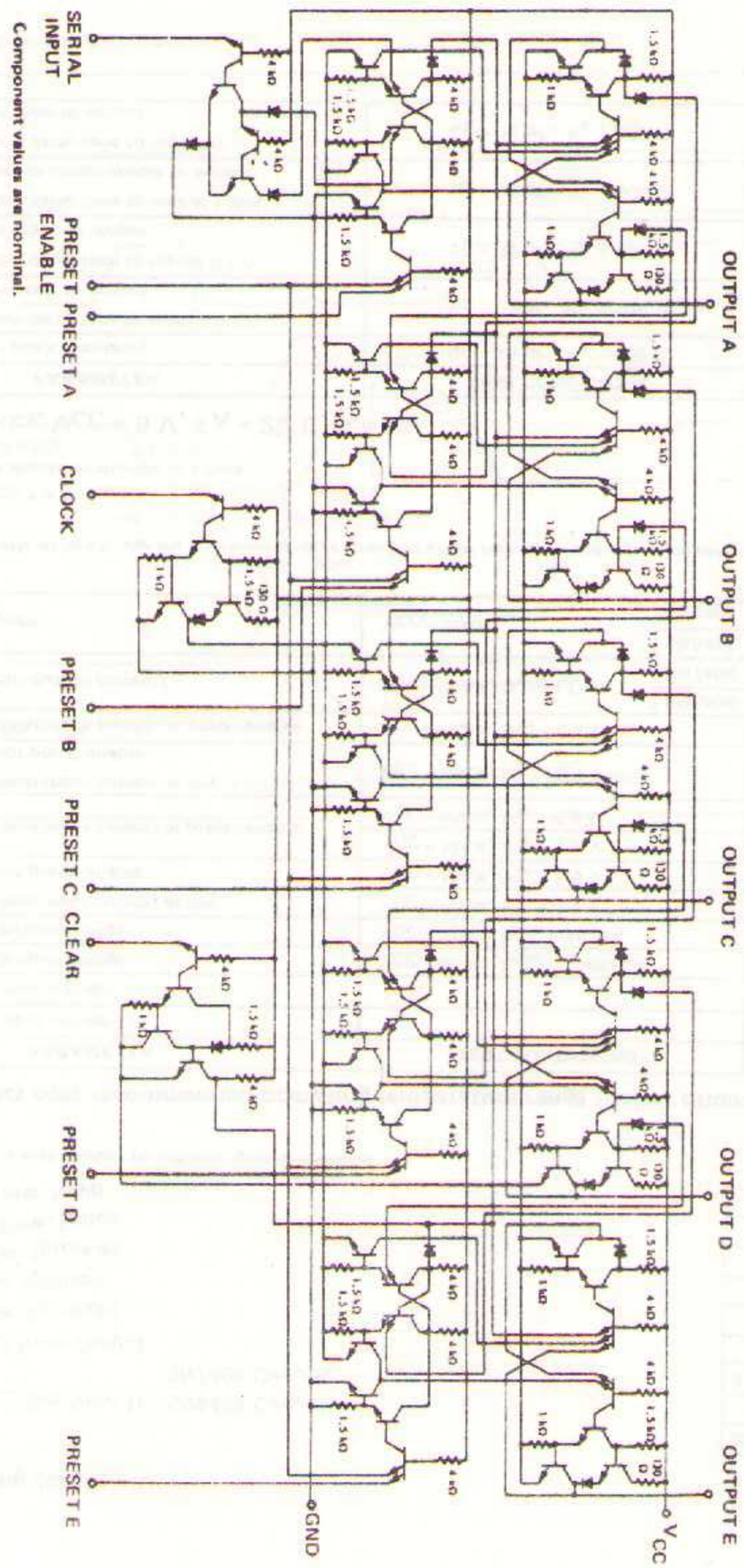
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω	10			MHz
t_{pd1}	Propagation delay time to logical 1 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd0}	Propagation delay time to logical 0 level from clock to output	C_L = 15 pF, R_L = 400 Ω		25	40	ns
t_{pd1}	Propagation delay time to logical 1 level from preset or preset-enable to output	C_L = 15 pF, R_L = 400 Ω		28	35	ns
t_{pd0}	Propagation delay time to logical 0 level from clear to output	C_L = 15 pF, R_L = 400 Ω			55	ns

functional block diagram

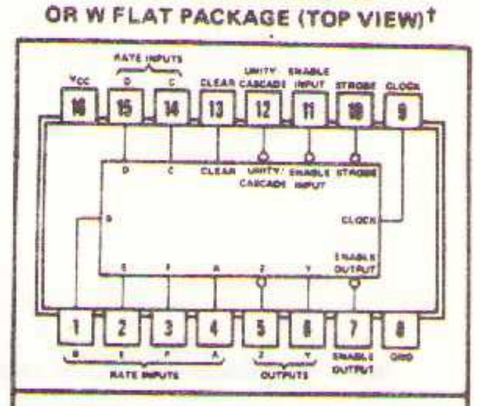




SN7497 . . . 6-BIT BINARY MULTIPLIER
SN74167 . . . DECADE MULTIPLIER

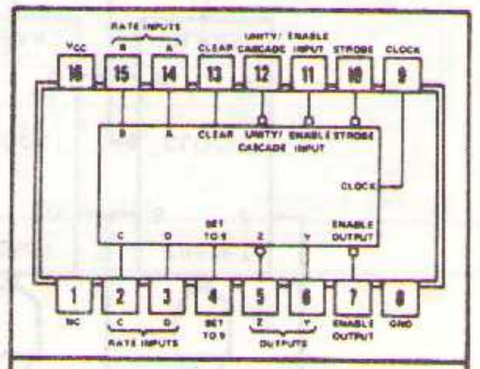
- **Perform Fixed-Rate or Variable-Rate Frequency Division**
- **For Applications in Arithmetic, Radar, Digital-to-Analog (D/A), Analog-to-Digital (A/D), and other Conversion Operations**
- **Typical Maximum Clock Frequency . . . 32 Megahertz**

SN7497
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

SN74167
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

NC—No internal connection

†Pin assignments for these circuits are the same for all packages.

description

These monolithic, fully synchronous, programmable counters utilize Series 54/74 TTL circuitry to achieve 32-megahertz typical maximum operating frequencies. The SN7497 is a six-bit serial binary counter; the SN74167 is a decade counter. These devices have buffered clock, clear, and enable inputs to control the operation of the counter, and a strobe input to enable or inhibit the rate input/decoding AND-OR-INVERT gates. The SN74167 also has a buffered set-to-nine input. The outputs have additional gating for cascading and transferring unity-count rates.

The counter is enabled when the clear, strobe, and enable inputs are low (for the decade counters, set-to-nine is also low). With the counter enabled the output frequency is equal to the input frequency multiplied by the rate input M and divided either by 64 (SN7497) or by 10 (SN74167), ie.:

$$\text{SN7497:} \quad f_{out} = \frac{M \cdot f_{in}}{64}$$

where: $M = F \cdot 2^5 + E \cdot 2^4 + D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$

$$\text{SN74167:} \quad f_{out} = \frac{M \cdot f_{in}}{10}$$

where: $M = D \cdot 2^3 + C \cdot 2^2 + B \cdot 2^1 + A \cdot 2^0$ for decimal zero through nine.

When the rate input is binary 0 (all rate inputs low), Z remains high. In order to cascade devices to perform 12-bit rate multiplication with the SN7497, or two-decade rate multiplication with the SN74167, the enable output is connected to the enable and strobe inputs of the next stage, the Z output of each stage is connected to the unity/cascade input of the other stage, and the sub-multiple frequency is taken from the Y output.

The unity/cascade input, when connected to the clock input, may be utilized to pass the clock frequency (inverted) to the Y output when the rate input/decoding gates are inhibited by the strobe. The unity/cascade input may also be used as a control for the Y output.

All of the inputs of these counters are diode-clamped, and each input, except the clock input, represents one normalized Series 54/74 load. The buffered clock input, used with the strobe gate, is only two Series 54/74 loads. Full fan-out to 10 Series 54/74 loads is available from each of the outputs. These devices are completely compatible with most TTL and DTL families. Typical power dissipation is 345 milliwatts for the SN7497, and 270 milliwatts for the SN74167. The SN7497 and SN74167 are characterized for operation from 0°C to 70°C.

description (continued)

SN7497

STATE AND/OR RATE TABLE (See Note A)

INPUTS										OUTPUTS			
			BINARY RATE							LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	F	E	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	L	L	64	H	L	H	1	C
L	L	L	L	L	L	L	L	H	64	H	1	1	1	C
L	L	L	L	L	L	L	H	L	64	H	2	2	1	C
L	L	L	L	L	L	H	L	L	64	H	4	4	1	C
L	L	L	L	L	H	L	L	L	64	H	8	8	1	C
L	L	L	L	H	L	L	L	L	64	H	16	16	1	C
L	L	L	H	L	L	L	L	L	64	H	32	32	1	C
L	L	L	H	H	H	H	H	H	64	H	63	63	1	C
L	L	L	H	H	H	H	H	H	64	L	H	63	1	E
L	L	L	H	L	H	L	L	L	64	H	40	40	1	F

SN74167

STATE AND/OR RATE TABLE (See Note A)

INPUTS										OUTPUTS			
			BCD RATE							LOGIC LEVEL OR NUMBER OF PULSES			
CLEAR	ENABLE	STROBE	D	C	B	A	NUMBER OF CLOCK PULSES	UNITY/ CASCADE	Y	Z	ENABLE	NOTES
H	X	H	X	X	X	X	X	H	L	H	H	B
L	L	L	L	L	L	L	10	H	L	H	1	C
L	L	L	L	L	L	H	10	H	1	1	1	C
L	L	L	L	L	H	L	10	H	2	2	1	C
L	L	L	L	L	H	H	10	H	3	3	1	C
L	L	L	L	H	L	L	10	H	4	4	1	C
L	L	L	L	H	L	H	10	H	5	5	1	C
L	L	L	L	H	H	L	10	H	6	6	1	C
L	L	L	L	H	H	H	10	H	7	7	1	C
L	L	L	H	L	L	L	10	H	8	8	1	C
L	L	L	H	L	L	H	10	H	9	9	1	C
L	L	L	H	L	H	L	10	H	8	8	1	C, D
L	L	L	H	L	H	H	10	H	9	9	1	C, D
L	L	L	H	H	L	L	10	H	8	8	1	C, D
L	L	L	H	H	L	H	10	H	9	9	1	C, D
L	L	L	H	H	H	L	10	H	8	8	1	C, D
L	L	L	H	H	H	H	10	H	9	9	1	C, D
L	L	L	H	L	L	H	10	L	H	9	1	E

NOTES: A. H = high level, L = low level, X = irrelevant. All remaining entries are numeric counts.

B. This is a simplified illustration of the clear function. The states of clock and strobe can affect the logic level of Y and Z. A low (L) unity/cascade will cause output Y to remain high.

C. Each rate illustrated assumes a constant value at rate inputs; however, these illustrations in no way prohibit variable-rate inputs.

D. These input conditions exceed the range of the decimal rate inputs.

E. Unity/cascade is used to inhibit output Y.

F. $f_{out} = \frac{M \cdot f_{in}}{64} = \frac{(8 + 32)\, f_{in}}{64} = \frac{40\, f_{in}}{64} = 0.625\, f_{in}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Normalized fan-out from output, N				10	
Input clock frequency, f_{clock}		0		25	MHz
Width of clock pulse, $t_{w(clock)}$		20			ns
Width of clear pulse, $t_{w(clear)}$		15			ns
Width of set-to-nine pulse $t_{w(set\text{-}to\text{-}9)}$	SN74167 (See Figure 1)	15			ns
Setup time, t_{setup}:					
From positive-going transition of clock pulse		25			ns
From negative-going transition of previous clock pulse		0		$t_{w(clock)}-10$	ns
Hold time, t_{hold}:	(See Figure 1)				
From positive-going transition of clock pulse		0		$t_{w(clock)}-10$	ns
From negative-going transition of previous clock pulse		0		$t_{cp}-10$	ns
Operating free-air temperature, T_A		0		70	C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH} High-level input voltage				2			V
V_{IL} Low-level input voltage						0.8	V
V_I Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA		2.4			V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH} High-level input current	clock input	V_{CC} = MAX, V_I = 2.4 V				80	μA
	other inputs					40	
I_{IL} Low-level input current	clock inputs	V_{CC} = MAX, V_I = 0.4 V				−3.2	mA
	other inputs					−1.6	
I_{OS} Short-circuit output current§		V_{CC} = MAX		−18		−55	mA
I_{CCH} Supply current, high-level output		V_{CC} = MAX, See Note 2	SN7497		58		mA
			SN74167		43		
I_{CCL} Supply current, low-level output		V_{CC} = MAX, See Note 3	SN7497		80	120	mA
			SN74167		65	99	

NOTES: 2. I_{CCH} is measured with outputs open and all inputs low.

3. I_{CCL} is measured with outputs open and all inputs high except the set-to-nine input of the SN74167, which is low.

†For test conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

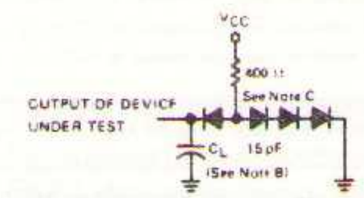
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	32		MHz
t_{PLH}	Enable	Enable			13	20	ns
t_{PHL}					14	21	
t_{PLH}	Strobe	Z			12	18	ns
t_{PHL}					15	23	
t_{PLH}	Clock	Y			26	39	ns
t_{PHL}					20	30	
t_{PLH}	Clock	Z			12	18	ns
t_{PHL}					17	26	
t_{PLH}	Rate	Z			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Unity/Cascade	Y			9	14	ns
t_{PHL}					6	10	
t_{PLH}	Strobe	Y			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clock	Enable			19	30	ns
t_{PHL}					22	33	
t_{PLH}	Clear	Y			24	36	ns
t_{PHL}		Z			15	23	
t_{PHL} (SN74167 only)	Set-to-9	Enable			18	27	ns
t_{PLH}	Any Rate Input	Y			15	23	ns
t_{PHL}					15	23	

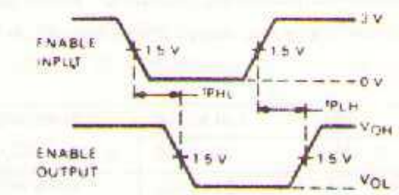
¶ f_{max} is maximum input clock frequency.
t_{PLH} is propagation delay time, low-to-high-level output.
t_{PHL} is propagation delay time, high-to-low-level output.

PARAMETER MEASUREMENT INFORMATION



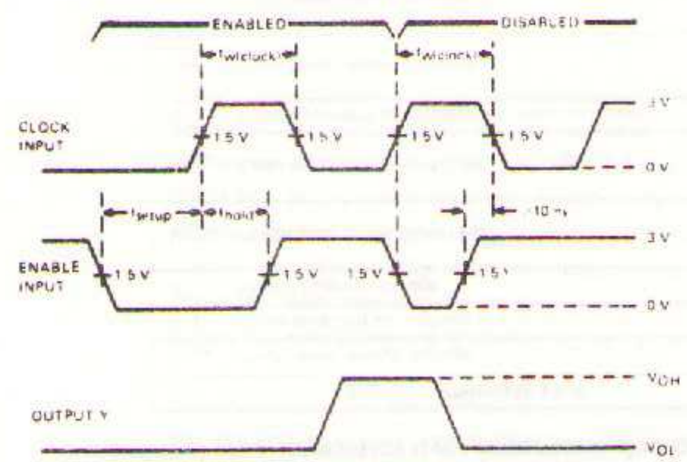
All three outputs are loaded during testing

LOAD CIRCUIT

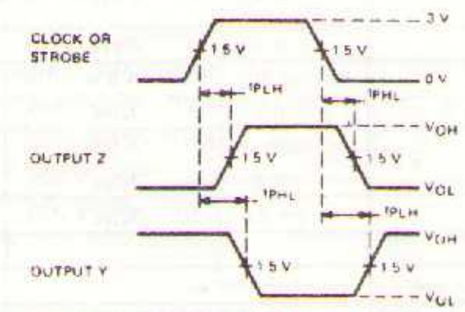


Flip-flops are at the maximum count. Other inputs are low.

PROPAGATION DELAY TIMES, ENABLE INPUT TO ENABLE OUTPUT

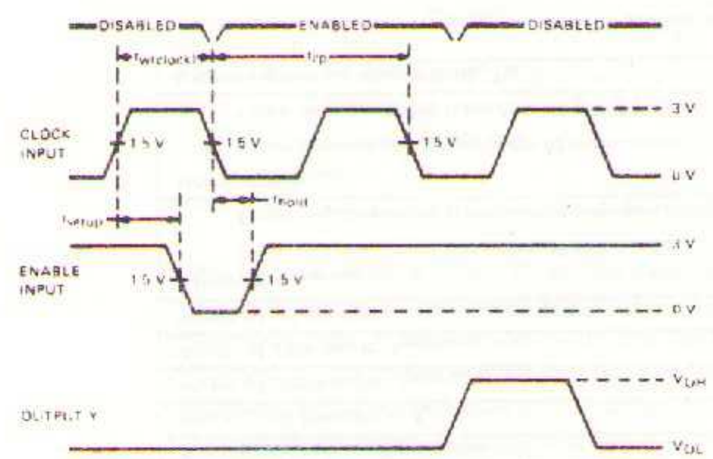


ENABLING FROM POSITIVE-GOING TRANSITION OF CLOCK PULSE

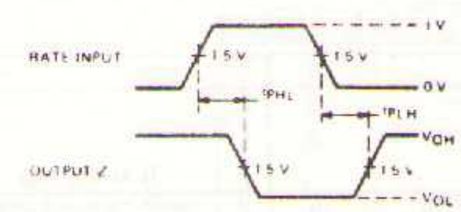


Unity/cascade and rate inputs are high, other inputs are low, and flip flops are at any count other than maximum.

PROPAGATION DELAY TIMES, CLOCK TO Z AND Y, AND STROBE INPUT TO Z AND Y

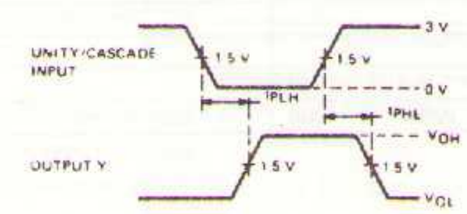


ENABLING FROM NEGATIVE-GOING TRANSITION OF PREVIOUS CLOCK PULSE



Flip-flops are at a count so that all other inputs to the gate under test are high all other inputs, including other rate inputs, are low.

PROPAGATION DELAY TIMES, RATE INPUT TO Z



Output Z is high.

PROPAGATION DELAY TIMES, UNITY/CASCADE INPUT TO Y

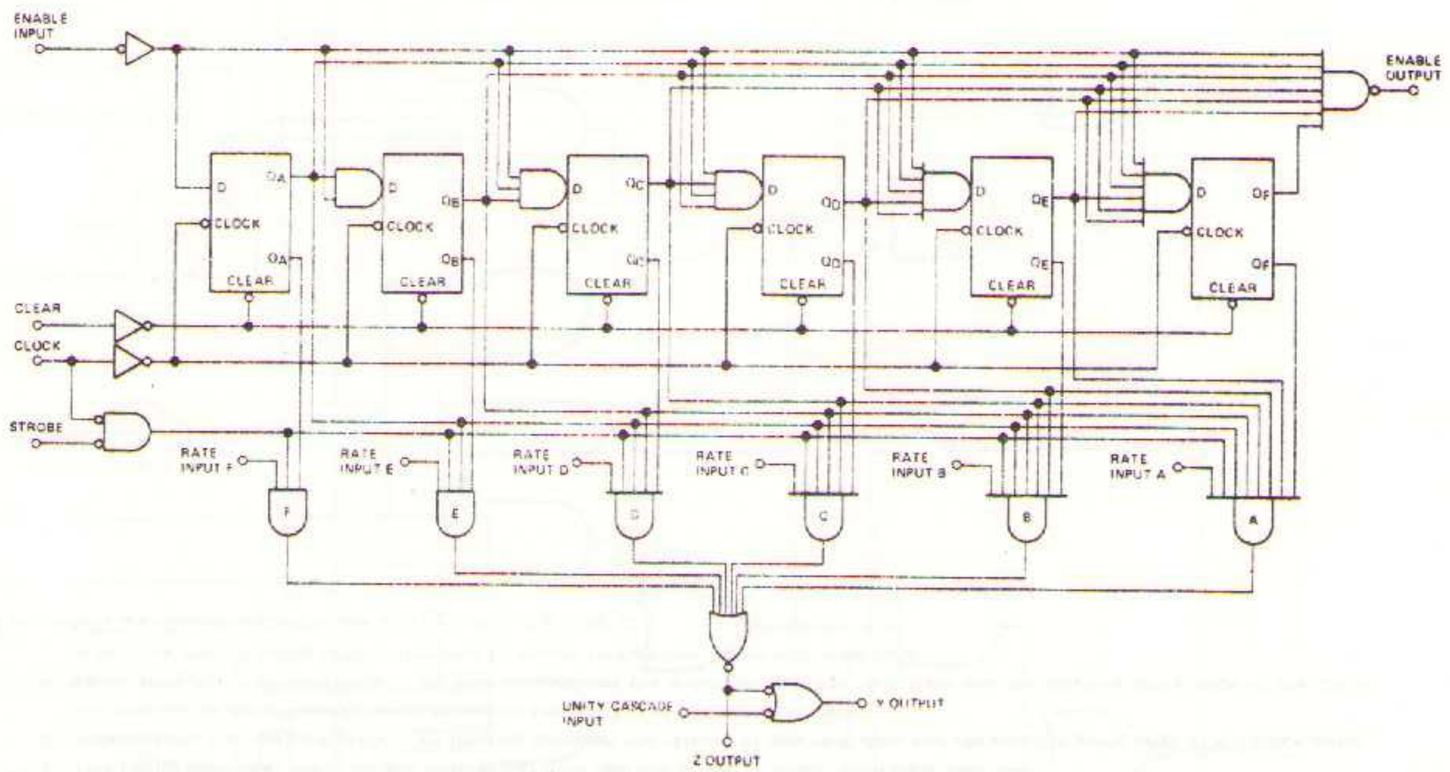
1. Unity/cascade and rate inputs are high, other inputs are low, and flip-flops are at any count other than maximum or one count before maximum.
2. Setup and hold times are illustrated for enabling a single clock pulse (count). Continued application of the enable function will enable subsequent clock pulses (counts) until disabling occurs (enable goes high). The total number of counts will be determined by the total number of positive-going clock transitions enabled.

NOTES: A. The input pulse generator has the following characteristics: $t_{w(clock)}$ = 20 ns, $t_{TLH} \leq$ 10 ns, $t_{THL} \leq$ 10 ns, PRR = 1 MHz, $Z_{out} \approx$ 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 1—SWITCHING TIMES

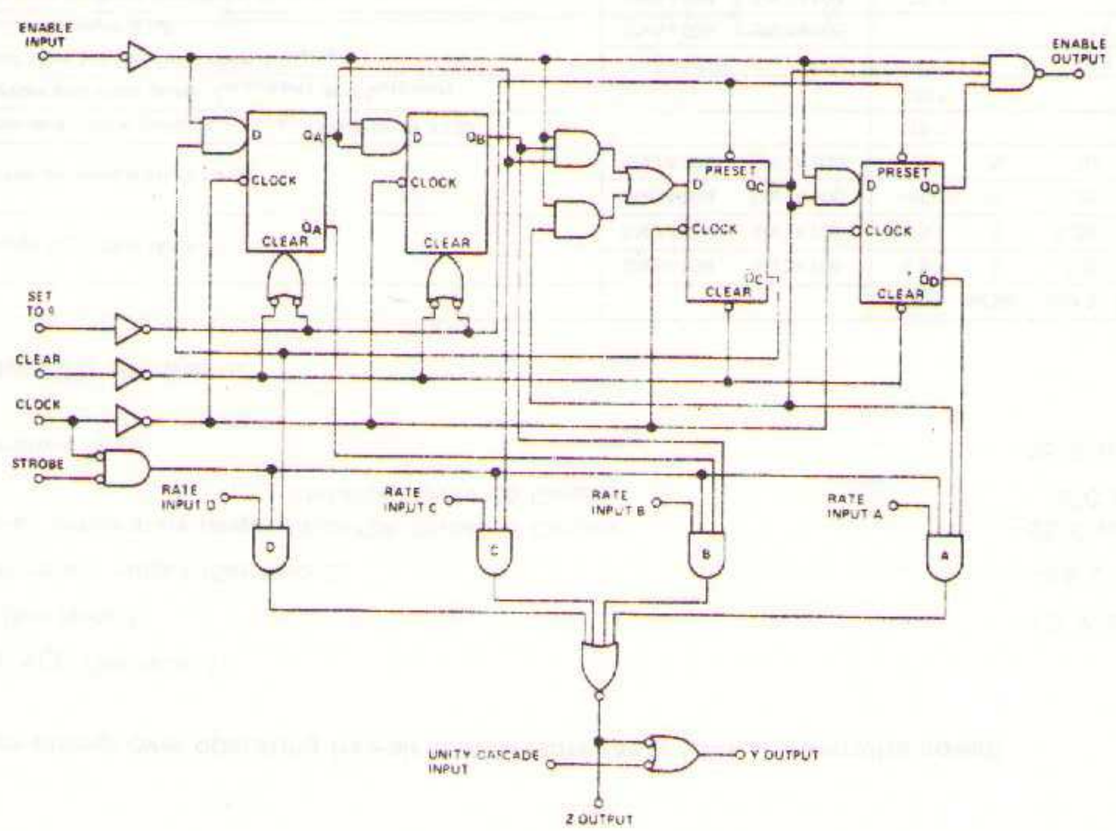
functional block diagram

SN7497 BINARY COUNTER



functional block diagram

SN74167 DECADE COUNTER



featuring

- Buffered Clock Input
- Direct Preset and Clear
- Common JK Gate Input

logic

TRUTH TABLE

INPUTS AT t_n			OUTPUTS AT t_{n+1}	
JK	J†	K†	Q	$\overline{Q}$
L‡	X	X	Q_n	$\overline{Q}_n$
H	L‡	L‡	Q_n	$\overline{Q}_n$
H	L	H	L	H
H	H	L	H	L
H	H	H	$\overline{Q}_n$	Q_n

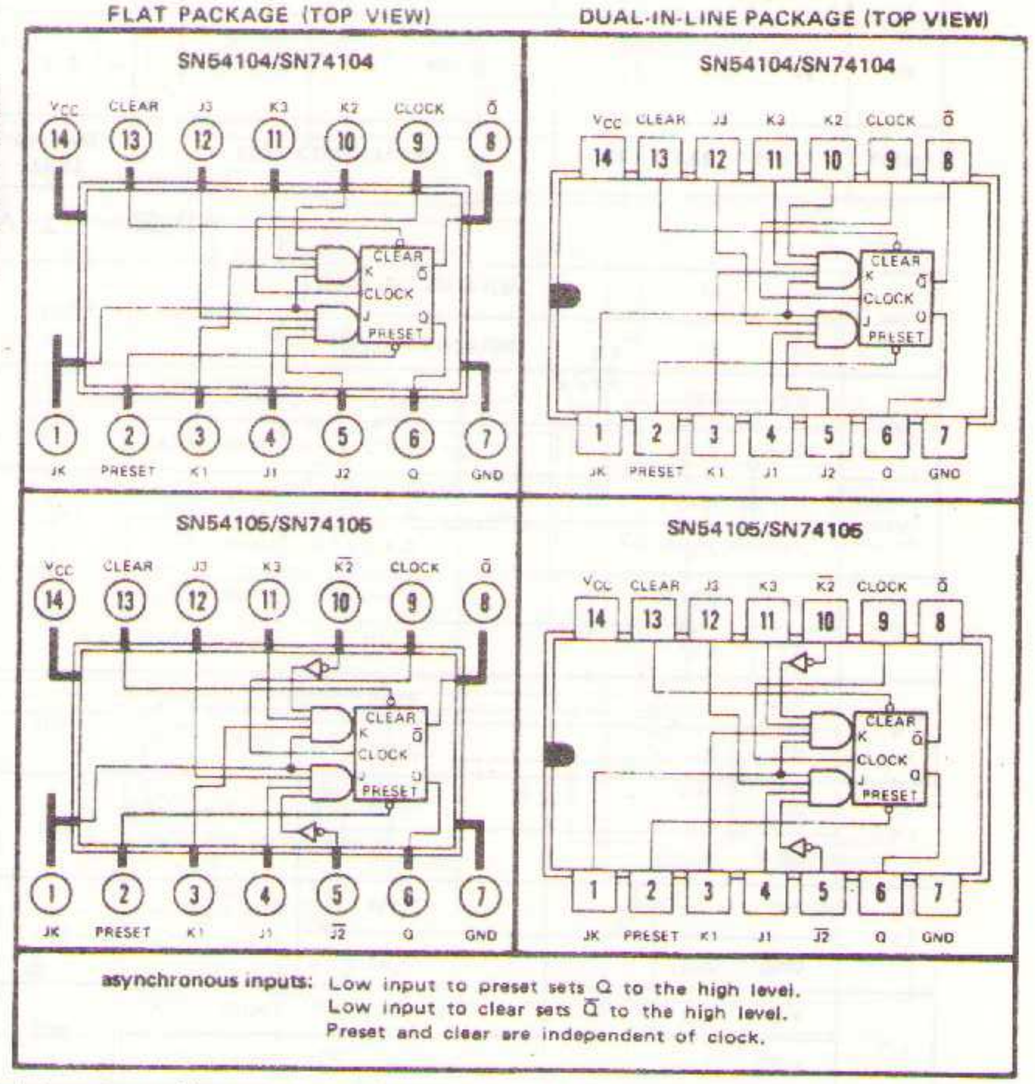
† SN54104/SN74104: $J = J1 \cdot J2 \cdot J3$, $K = K1 \cdot K2 \cdot K3$
SN54105/SN74105: $J = J1 \cdot \overline{J2} \cdot J3$, $K = K1 \cdot \overline{K2} \cdot K3$

‡ These low levels must be maintained while the clock is low

NOTES:
A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
C. H = high, L = low, X = irrelevant.

W
FLAT PACKAGE (TOP VIEW)

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



asynchronous inputs: Low input to preset sets Q to the high level.
Low input to clear sets Q̄ to the high level.
Preset and clear are independent of clock.

description

These J-K master-slave flip-flops feature a buffered clock input, direct preset and clear, gated J and K inputs, and a common JK input. The clock buffer offers typical TTL high noise immunity, low clock-line loading, and, in most cases, eliminates the need for stringent control of system-clock rise and fall times. When activated, the direct preset and clear inputs control the state of both the master and slave flip-flops independent of the clock and synchronous-input states. Gated inputs may be used to perform a wide variety of control functions without the need for external gates, and the common JK input simplifies hardware design for applications utilizing a single gate-control source.

Due to the internal clock buffer, the JK input gates accept data when the clock line is low, and transfer of data from the master to the slave occurs during the clock-line transition from the low state to the high state. When the clock line is high, the data inputs are inhibited.

The SN54104/SN74104 includes internal capacitive loading on the J and K input gates and, as the input setup and hold times are lengthened, this circuit displays improved performance in systems where appreciable clock skew is anticipated.

The SN54105/SN74105 offers an inverting data input to each of the J and K input gates for additional control flexibility. As the input setup and hold times are not lengthened, this circuit permits operation at higher toggle rates than the SN54104/SN74104.

These TTL circuits feature one-volt typical d-c noise margins and are compatible for use with most TTL and DTL families. Full fan-out to 10 normalized Series 54/74 loads is available from the outputs. The SN54104 and SN54105 circuits are characterized for operation over the full military temperature range of −55°C to 125°C, and the SN74104 and SN74105 circuits are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (See Note 1) . . . . . 8 V

Input voltage (See Note 1) . . . . . −1.5 V to 5.5 V

Voltage applied to any output (See Note 2) . . . . . −0.5 V to V_{CC}

Operating free-air temperature range: SN54104, SN54105 Circuits . . . . . −55°C to 125°C

SN74104, SN74105 Circuits . . . . . 0°C to 70°C

Storage temperature range . . . . . −65°C to 150°C

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (See Note 1)	SN54104, SN54105	4.5	5	5.5	V
	SN74104, SN74105	4.75	5	5.25	
Operating free-air temperature range	SN54104, SN54105	−55	25	125	°C
	SN74104, SN74105	0	25	70	
Width of low-level clock pulse, $t_{w(clock)}$ (See Figure 112)		15†			ns
Width of preset and clear pulse, $t_{w(preset)}$ and $t_{w(clear)}$		20†			ns
Input release time for low-level data, $t_{release(L)}$ (See Note 3 and Figure 113)	SN54104, SN74104			10†	ns
	SN54105, SN74105			1†	
Input setup time for high-level data, $t_{setup(H)}$ (See Note 4 and Figure 113)	SN54104, SN74104	35†			ns
	SN54105, SN74105	10†			

NOTES: 1. Voltage values are with respect to network ground terminal.

2. This rating applied at the Q output with preset held low and at the $\overline{Q}$ output with clear held low.

3. Release time for low-level data is an interval between the release of low-level data and the positive-going edge of the clock pulse, this interval being sufficiently short to ensure recognition of the low-level data.

4. Setup time for high-level data is an interval between the arrival of the high-level data and the positive-going edge of the clock pulse, this interval being sufficiently long to ensure recognition of the high-level data.

†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	107 and 108		T_A = MIN	2			V
				T_A = 25°C	1.7			
				T_A = MAX	1.4			
V_{IL}	Low-level input voltage	107 and 108		T_A = MIN			0.8	V
				T_A = 25°C			0.9	
				T_A = MAX			0.8	
V_{OH}	High-level output voltage	107	V_{CC} = MIN,	I_{OH} = −1 mA	2.4	2.7		V
V_{OL}	Low-level output voltage	108	V_{CC} = MAX,	I_{OL} = 17.7 mA		0.2	0.4	V
			V_{CC} = MIN,	I_{OL} = 16 mA		0.2	0.4	
I_{IH}	High-level input current into any input except JK, preset, or clear	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		2	40	μA
				T_A = MAX			40	
I_{IH}	High-level input current into JK	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		4	80	μA
				T_A = MAX			80	
I_{IH}	High-level input current into preset or clear	109	V_{CC} = MAX, V_I = 4.5 V	T_A = 25°C		8	120	μA
				T_A = MAX			120	
I_{IL}	Low-level input current into any input except JK, preset, or clear	110	V_{CC} = MAX	V_I = 0.4 V		−1.1	−1.6	mA
			V_{CC} = MIN	V_I = 0.4 V		−0.9	−1.45	
I_{IL}	Low-level input current into JK	110	V_{CC} = MAX,	V_I = 0.4 V		−2.2	−3.2	mA
			V_{CC} = MIN,	V_I = 0.4 V		−1.8	−2.9	
I_{IL}	Low-level input current into preset or clear	110	V_{CC} = MAX,	V_I = 0.4 V		−3	−4.75	mA
			V_{CC} = MIN,	V_I = 0.4 V		−2.5	−3.9	
I_{CC}	Supply current	111	V_{CC} = 5 V	SN54104, SN74104		15	24	mA
				SN54105, SN74105		17	28	

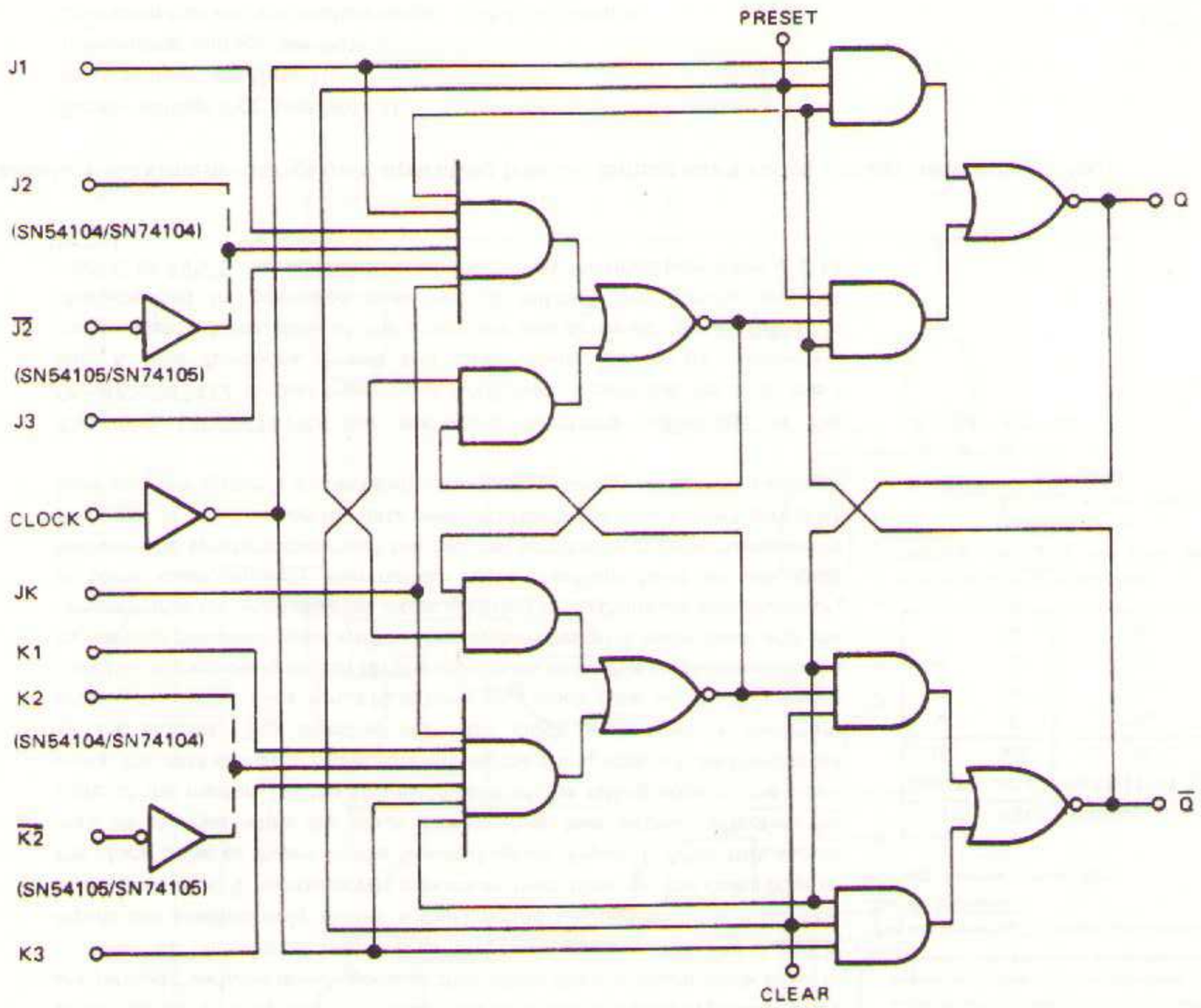
switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		9	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from clock	112	C_L = 15 pF, R_L = 400 Ω		16	25	ns

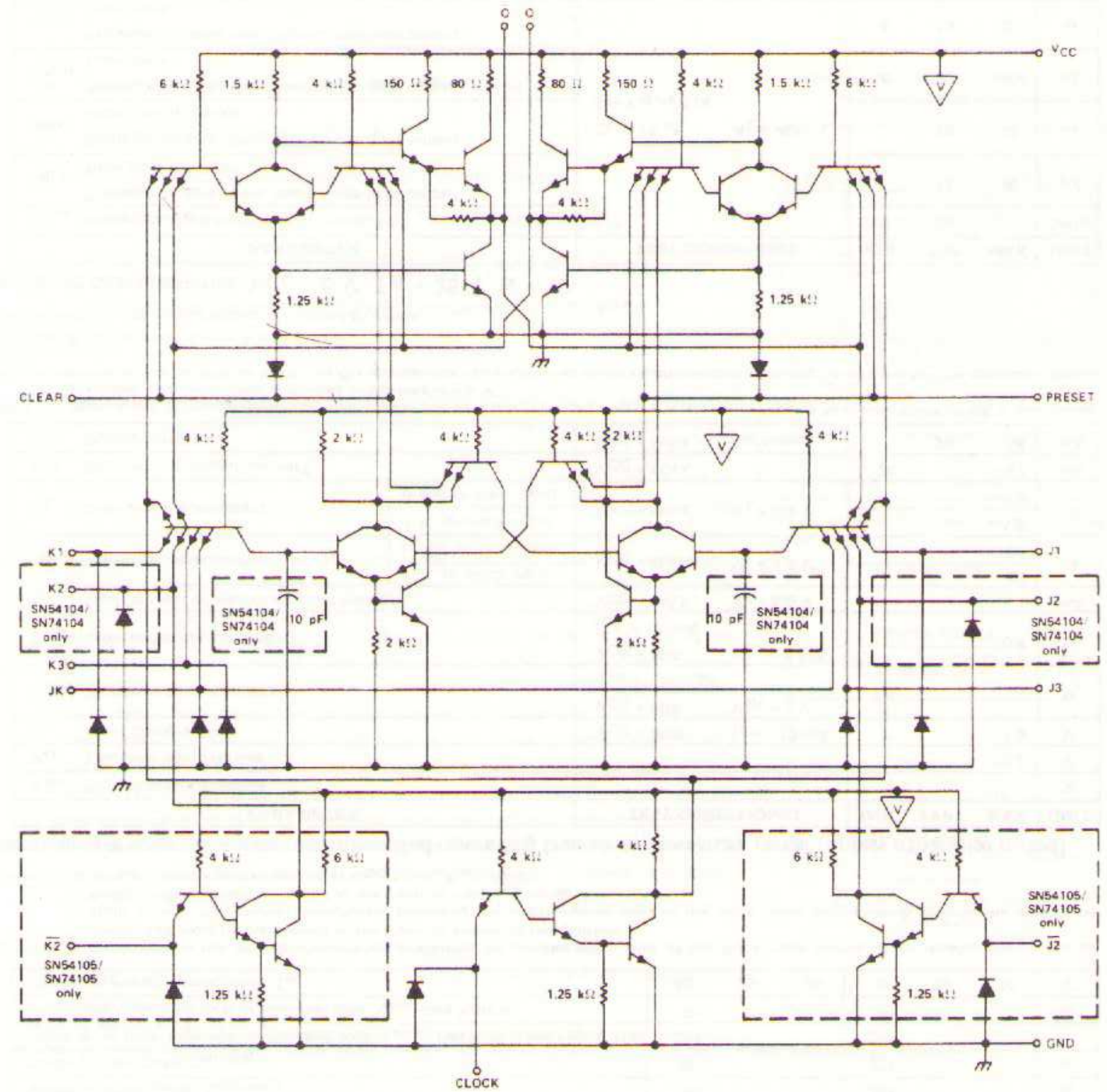
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

functional block diagram



schematic



Component values shown are nominal.

▽ ... V_{CC} bus

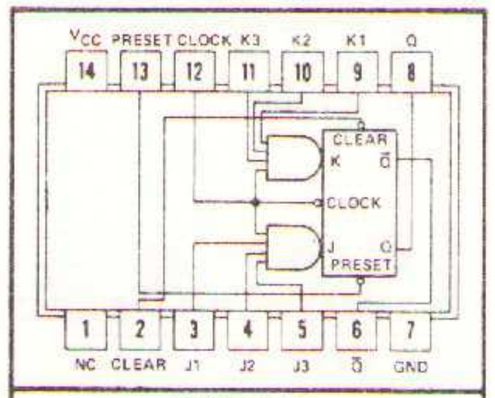
- Data Lockout Solves Clock-Skew Problems
- Improved Immunity to Noise
- Input-Clamping Diodes Simplify System Design
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits
- Typical Maximum Input Clock Frequency . . . 25 MHz

description

The SN54110 and SN74110 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled only during a short period (20 nanoseconds maximum setup time plus 5 nanoseconds maximum hold time) on the rising edge of the clock pulse as shown in the timing diagram, Figure 1. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. On the threshold level of the falling edge of the clock pulse, the data stored in the master during the rising edge will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptability to noise is thereby effectively reduced.

The SN54110/SN74110 has the same functional advantage as the SN5472/SN7472 in that three-input AND logic is provided for both the J and K data functions. Preset and clear inputs, which are completely independent of the state of the clock, are also provided. The SN54110 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74110 is characterized for operation from 0°C to 70°C.

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

†Pin assignments for these circuits are the same for all packages.
NC—No internal connection.

TRUTH TABLE

INPUTS AT t_n		OUTPUT AT t_{n+1}
J‡	K‡	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = high level, L = low level
NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.
‡J = J1 • J2 • J3
K = K1 • K2 • K3

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54110 Circuits	−55°C to 125°C
SN74110 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the J input with respect to clear and clock, and to the K input with respect to preset and clock.

recommended operating conditions

		SN54110			SN74110			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		20†	0		20†	MHz
Width of clock pulse, $t_{w(clock)}$		25†			25†			ns
Width of preset pulse, $t_{w(preset)}$		25†			25†			ns
Width of clear pulse, $t_{w(clear)}$		25†			25†			ns
Input setup time, high-level or low-level data, t_{setup} (see Note 3 and Figure 114)		20†			20†			ns
Input hold time, high-level or low-level data, t_{hold} (see Note 4)		5†			5†			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to insure its recognition.
†These conditions are recommended for use at V_{CC} = 5 V, T_A = 25°C.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

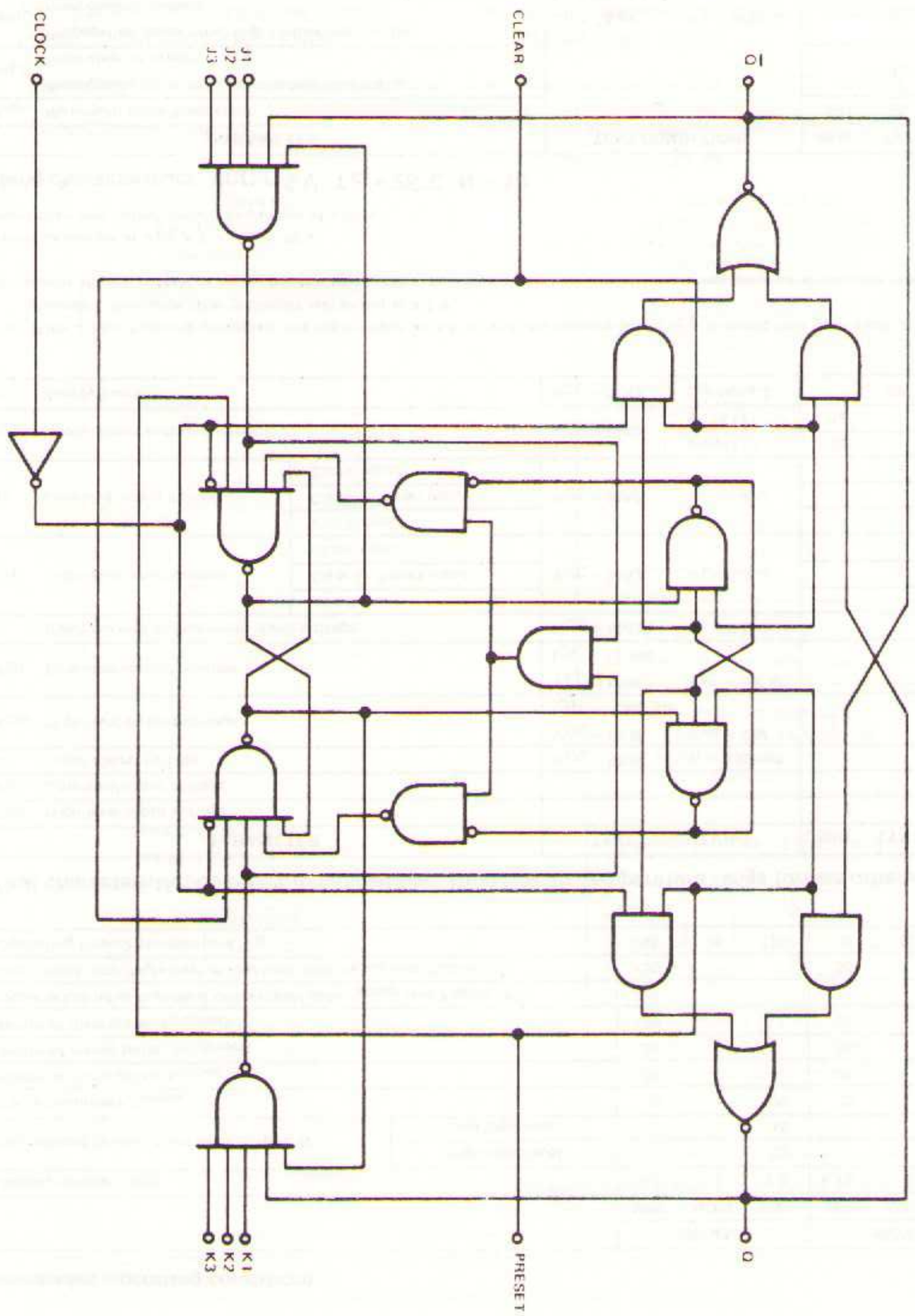
PARAMETER		TEST CONDITIONS‡		MIN	TYP§	MAX	UNIT
V_{IH} High-level input voltage				2			V
V_{IL} Low-level input voltage						0.8	V
V_I Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, I_{OH} = −800 μA	V_{IH} = 2 V,	2.4			V
V_{OL} Low-level output voltage		V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH} High-level input current	J, K, or clock input	V_{CC} = MAX,	V_I = 2.4 V			40	μA
	preset or clear input					160	
I_{IL} Low-level input current	J, K, or clock input	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
	preset or clear input					−3.2	
I_{OS} Short-circuit output current¶		V_{CC} = MAX		−20		−57	mA
I_{CC} Supply current		V_{CC} = MAX,	See Note 5		20	34	mA

NOTE 5: With J and K inputs grounded, the clock input at 4.5 V, and the outputs open, I_{CC} is tested first with clear at 4.5 V and preset grounded, then with clear grounded and preset at 4.5 V.
‡For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§All typical values are at V_{CC} = 5 V, T_A = 25°C.
¶Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

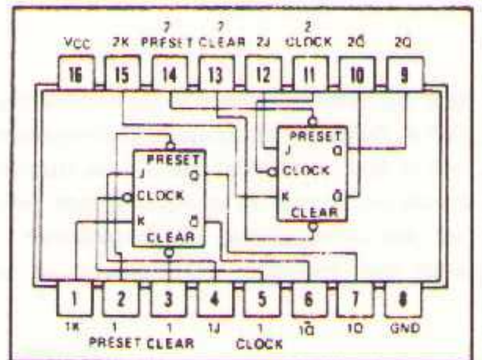
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 114	20	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			12	20	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			18	25	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		10	20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		6	13	20	ns

dual j-k master-slave flip-flops with data lockout



- Data Lockout Solves Clock-Skew Problems
- Improved Immunity to Noise
- Input-Clamping Diodes Simplify System Design
- High-Fan-Out, Low-Impedance, Totem-Pole Outputs
- Fully Compatible with Most TTL, DTL, and MSI Circuits
- Typical Maximum Input Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic:
Low input to preset sets Q to high level
Low input to clear resets Q to low level
Preset and clear are independent of clock

†Pin assignments for these circuits are the same for all packages.

description

The SN54111 and SN74111 are d-c coupled, variable-skew, J-K flip-flops which utilize TTL circuitry to obtain 25-MHz performance typically. They are termed "variable-skew" because they allow the maximum clock skew in a system to be a direct function of the clock pulse width. The J and K inputs are enabled to accept data only during a short period (30 nanoseconds maximum hold time) starting with, and immediately following, the rising edge of the clock pulse as shown in the timing diagram, Figure 1. After this, inputs may be changed while the clock is at the high level without affecting the state of the master. At the threshold level of the falling edge of the clock pulse, the data stored in the master will be transferred to the output. The effective allowable clock skew then is minimum propagation delay time minus hold time, plus clock pulse width. This means that the system designer can set the maximum allowable clock skew needed by varying the clock pulse width. Thus system design is made easier and the requirements for sophisticated clock distribution systems are minimized or, in some cases, entirely eliminated. These flip-flops have an additional feature—the synchronous input has reduced sensitivity to data change while the clock is high because the data need be present for only a short period of time and the system's susceptibility to noise is thereby effectively reduced.

The SN54111 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74111 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS AT t_n		OUTPUT AT t_{n+1}
J	K	Q
L	L	Q_n
L	H	L
H	L	H
H	H	$\bar{Q}_n$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse.
B. t_{n+1} = bit time after clock pulse.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54111 Circuits	−55°C to 125°C
SN74111 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the J input with respect to clear and clock, and to the K input with respect to preset and clock.

recommended operating conditions

		SN54111			SN74111			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of preset pulse, $t_{w(preset)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		25			25			ns
Input setup time, high-level or low-level data, t_{setup} (see Figure 115)		0			0			ns
Input hold time, high-level or low-level data, t_{hold} (see Figure 115)		30			30			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	J or K input	V_{CC} = MAX, V_I = 2.4 V				40	μA
		Clear or Preset input					80	
		Clock input					120	
I_{IL}	Low-level input current	J or K input	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
		Clear or Preset input					−3.2	
		Clock input					−4.8	
I_{OS}	Short-circuit output current §		V_{CC} = MAX	SN54111	−20		−57	mA
				SN74111	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX,	See Note 3		28	41	mA

NOTE 3: With J and K inputs grounded, the clock input at 4.5 V, and the outputs open, I_{CC} is tested first with clear at 4.5 V and preset grounded, then with clear grounded and preset at 4.5 V.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

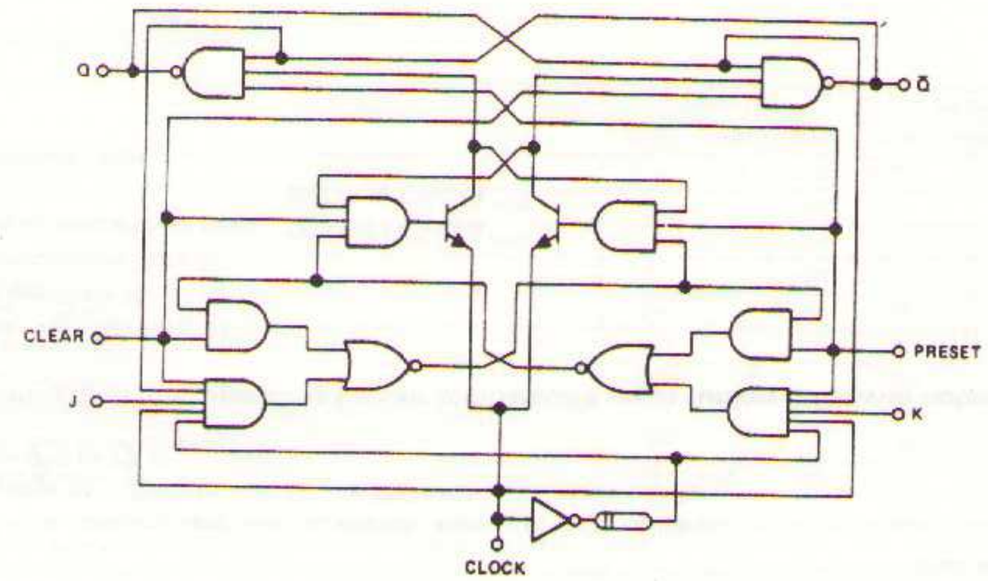
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 115	20	25		MHz
t_{PLH}	Propagation delay time, low-to-high-level output from clear or preset			12	18	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear or preset			21	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		6	12	17	ns
t_{PHL}	Propaagtion delay time, high-to-low-level output from clock		10	20	30	ns

functional block diagram (each flip-flop)



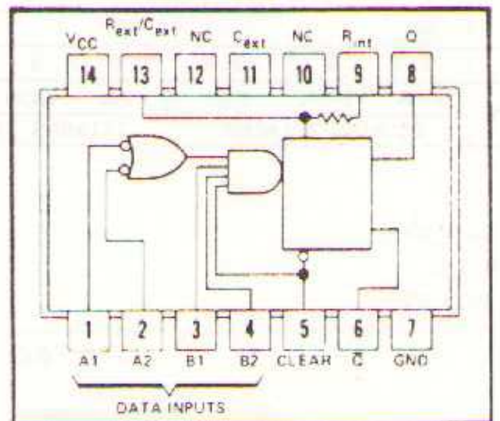
- Retriggerable for Very Long Output Pulses, Up to 100% Duty Cycle
- Overriding Clear Terminates Output Pulse
- Diode-Clamped Inputs
- D-C Triggered from High- or Low-Level Gated Logic Inputs
- Compatible for Use with TTL or DTL
- Typical Average Propagation Delay to Output Q . . . 21 ns

logic

SN54122, SN74122
TRUTH TABLE
(See Note A)

INPUTS				OUTPUTS	
A1	A2	B1	B2	Q	$\overline{Q}$
H	H	X	X	L	H
X	X	L	X	L	H
X	X	X	L	L	H
L	X	H	H	L	H
L	X	↑	H	⎍	⎏
L	X	H	↑	⎍	⎏
X	L	H	H	L	H
X	L	↑	H	⎍	⎏
X	L	H	↑	⎍	⎏
H	↓	H	H	⎍	⎏
↓	↓	H	H	⎍	⎏
↓	H	H	H	⎍	⎏

SN54122, SN74122
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†
(SEE NOTES B THRU D)

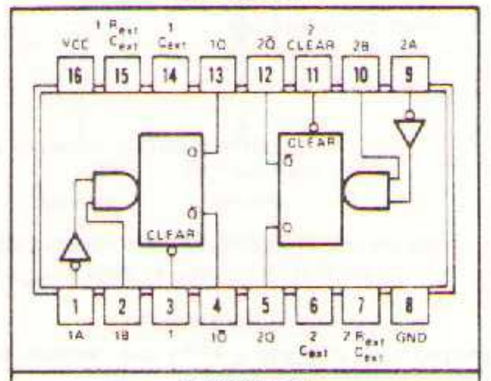


positive logic:
Low input to clear resets Q to low level and inhibits data inputs

SN54123, SN74123
TRUTH TABLE
(See Note A)

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎏
↓	H	⎍	⎏

SN54123, SN74123
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†
(SEE NOTE D)



positive logic:
Low input to clear resets Q to low level and inhibits data inputs

†Pin assignments for these circuits are the same for all packages.

NOTES: A. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎏ = one low-level pulse, X = irrelevant (any input, including transitions).
B. NC = No internal connection.
C. To use the internal timing resistor of SN54122/SN74122 (10 kΩ nominal), connect R_{int} to V_{CC}.
D. An external timing capacitor may be connected between C_{ext} and R_{ext}/C_{ext} (positive).

description

These monolithic TTL retriggerable monostable multivibrators feature d-c triggering from gated low-level-active (A) and high-level-active (B) inputs, and also provide overriding direct clear inputs. Complementary outputs are provided. A full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs at the low logic level, and in the high-level state, a fan-out of 20 is available. The retrigger capability simplifies the generation of output pulses of extremely long duration. By triggering the input before the output pulse is terminated, the output pulse may be extended. The overriding clear capability permits any output pulse to be terminated at a predetermined time independently of the timing components R and C.

Figure A below illustrates triggering the one-shot with the high-level-active (B) inputs.

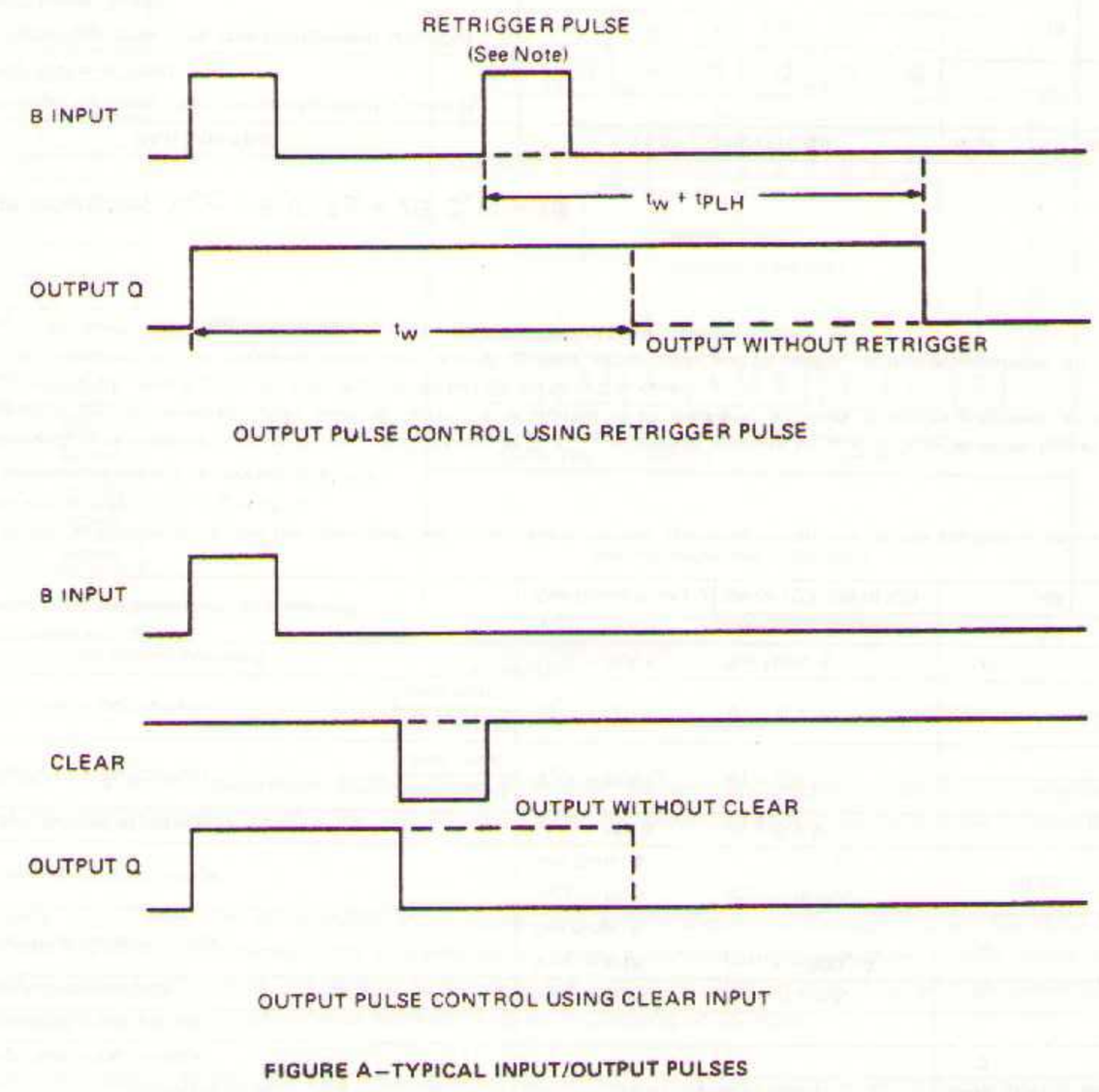


FIGURE A—TYPICAL INPUT/OUTPUT PULSES

NOTE: Retrigger pulse must not start before 0.22 C_{ext} (in picofarads) nanoseconds after previous trigger pulse.

description (continued)

These monostables are designed to provide the system designer with complete flexibility in controlling the pulse width, either to lengthen the pulse by retriggering, or to shorten by clearing. SN54122/SN74122 has an internal timing resistor which allows the circuit to be operated with only an external capacitor, if so desired. Applications requiring more precise pulse widths and not requiring the clear feature can best be satisfied with SN54121/SN74121.

The output pulse is primarily a function of the external capacitor and resistor. For $C_{ext} > 1000$ pF, the output pulse width (t_w) is defined as:

$$t_w = 0.32\, R_T C_{ext} \left(1 + \frac{0.7}{R_T}\right)$$

where

R_T is in kΩ (either internal or external timing resistor)
C_{ext} is in pF
t_w is in ns

For pulse widths when $C_{ext} \leq 1000$ pF, see Figure 3.

These circuits are fully compatible with most TTL or DTL families. Inputs are diode-clamped to minimize reflections due to transmission-line effects, which simplifies design. Typical power dissipation per one shot is 115 milliwatts; typical average propagation delay time to the Q output is 21 nanoseconds. The SN54122 and SN54123 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74122 and SN74123 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage, SN54122, SN74122 Circuits only (see Note 2)	5.5 V
Operating free-air temperature range: SN54122, SN54123 Circuits	−55°C to 125°C
SN74122, SN74123 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

		SN54122, SN54123			SN74122, SN74123			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input data setup time, t_{setup} (see Note 3 and Figure 116)		40†			40†			ns
Input data hold time, t_{hold} (see Note 4 and Figure 116)		40†			40†			ns
Width of clear pulse, $t_{w(clear)}$		40†			40†			ns
External timing resistance		5		25	5		50	kΩ
External capacitance		No restriction			No restriction			
Wiring capacitance at R_{ext}/C_{ext} terminal				50			50	pF
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

† These conditions are recommended for use at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For the SN54122/SN74122 circuit, this rating applies to each A input with respect to the other and to each B input with respect to the other.
3. Setup time for a dynamic input is the interval immediately preceding the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure recognition of the transition.
4. Hold time for a dynamic input is the interval immediately following the transition which constitutes the dynamic input, during which interval a steady-state logic level must be maintained at the input to ensure continued recognition of the transition.

electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN,	I_I = −12 mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, See Note 5	I_{OH} = −800 μA,	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, See Note 5	I_{OL} = 16 mA,		0.22	0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	data inputs	V_{CC} = MAX,	V_I = 2.4 V			40	μA
		clear input					80	
I_{IL}	Low-level input current	data inputs	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
		clear input					−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX,	See Note 5	−10		−40	mA
I_{CC}	Supply current (quiescent or triggered)		V_{CC} = MAX, See Notes 6 and 7	SN54122, SN74122		23	28	mA
				SN54123, SN74123		46	66	

† For conditions shown as MIN or MAX, use the value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.
§ Not more than one output should be shorted at a time.

NOTES: 5. Ground C_{ext} to measure V_{OH} at Q, V_{OL} at $\overline{Q}$, or I_{OS} at Q. C_{ext} is open to measure V_{OH} at $\overline{Q}$, V_{OL} at Q, or I_{OS} at $\overline{Q}$.
6. Quiescent I_{CC} is measured (after clearing) with 2.4 V applied to all clear and A inputs, B inputs grounded, all outputs open, C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of SN54122/SN74122 is open.
7. I_{CC} is measured in the triggered state with 2.4 V applied to all clear and B inputs, A inputs grounded, all outputs open C_{ext} = 0.02 μF, and R_{ext} = 25 kΩ. R_{int} of SN54122/SN74122 is open.

switching characteristics, $V_{CC} = 5$ V, $T_A = 25°C$, N = 10

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either A input	C_{ext} = 0, C_L = 15 pF, See Figure 116	R_{ext} = 5 kΩ, R_L = 400 Ω,		22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output, from either B input				19	28	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either A input				30	40	ns
t_{PHL}	Propagation delay time, high-to-low-level $\overline{Q}$ output, from either B input				27	36	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output, from clear input				18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level $\overline{Q}$ output, from clear input				30	40	ns
$t_{w(min)}$	Minimum width of Q output pulse				45	65	ns
t_w	Width of Q output pulse	C_{ext} = 1000 pF, C_L = 15 pF,	R_{ext} = 10 kΩ, R_L = 400 Ω	3.08	3.42	3.76	μs

TYPICAL CHARACTERISTICS

OUTPUT PULSE WIDTH
vs
EXTERNAL TIMING CAPACITANCE

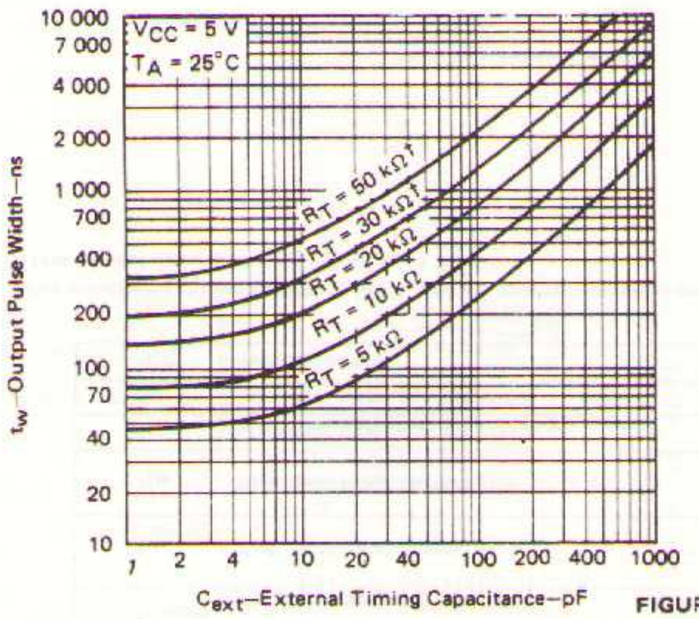
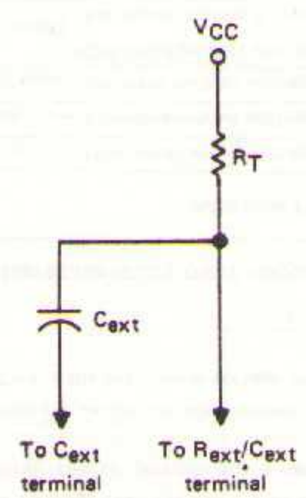


FIGURE B

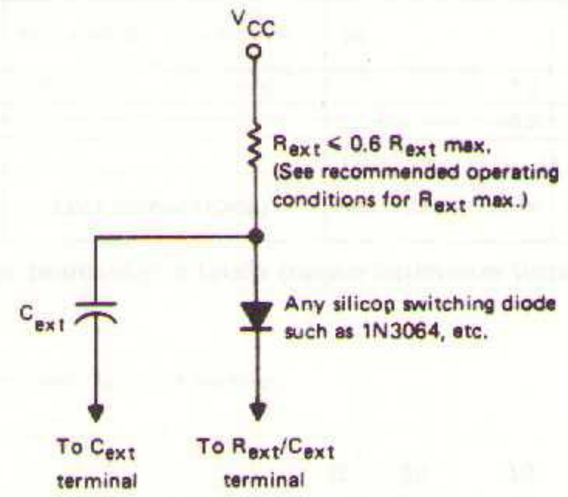
†These values of resistance exceed the maximums recommended for use over the full temperature range of the SN54122 and SN54123.

TYPICAL APPLICATION DATA



TIMING COMPONENT CONNECTIONS WHEN C_{ext} < 1000 pF

FIGURE C



TIMING COMPONENT CONNECTIONS WHEN C_{ext} > 1000 pF AND CLEAR IS USED

FIGURE D

To prevent reverse voltage across C_{ext}, it is recommended that the method shown in Figure D be employed when using electrolytic capacitors and in applications utilizing the clear function. In all applications using the diode, the pulse width is:

$$t_w = 0.28\ R_{ext}C_{ext}\left(1 + \frac{0.7}{R_{ext}}\right)$$

where R_{ext} is in kΩ
C_{ext} is in pF
t_w is in ns

- **Drives gas-filled cold-cathode indicator tubes directly**
- **Fully decoded inputs ensure all outputs are off for invalid codes**
- **Input clamping diodes minimize transmission-line effects**
- **Power dissipation typically 55 mW**

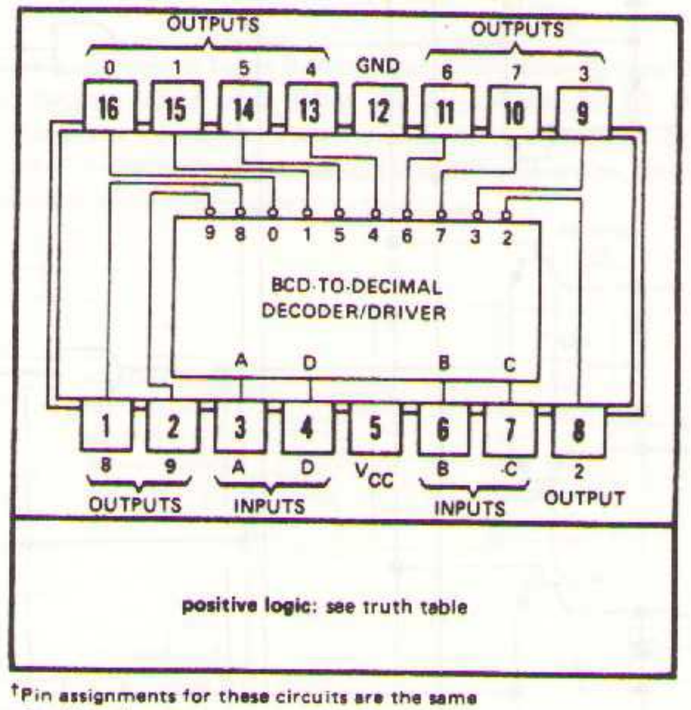
logic

TRUTH TABLE

INPUT				OUTPUT
D	C	B	A	ON†
L	L	L	L	0
L	L	L	H	1
L	L	H	L	2
L	L	H	H	3
L	H	L	L	4
L	H	L	H	5
L	H	H	L	6
L	H	H	H	7
H	L	L	L	8
H	L	L	H	9
H	L	H	L	NONE
H	L	H	H	NONE
H	H	L	L	NONE
H	H	L	H	NONE
H	H	H	L	NONE
H	H	H	H	NONE

H = high level, L = low level
†All other outputs are off

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

The SN74141 is a second-generation BCD-to-decimal decoder designed specifically to drive cold-cathode indicator tubes. This decoder demonstrates an improved capability to minimize switching transients in order to maintain a stable display.

Full decoding is provided for all possible input states. For binary inputs 10 through 15, all the outputs are off. Therefore the SN74141, combined with a minimum of external circuitry, can use these invalid codes in blanking leading- and/or trailing-edge zeros in a display as shown in the typical application data. The ten high-performance, n-p-n output transistors have a maximum reverse current of 50 microamperes at 55 volts.

Low-forward-impedance diodes are also provided for each input to clamp negative-voltage transitions in order to minimize transmission-line effects. Power dissipation is typically 55 milliwatts, which is about one-half the power requirement of earlier designs. The SN74141 is characterized for operation over the temperature range of 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC}	7 V
Input voltage (see Note 1)	5.5 V
Current into any output (off-state)	2 mA
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage V_{CC} (see Note 1)	4.75	5	5.25	V
Output voltage (see Notes 1 and 2)			65	V
Operating free-air temperature range	0	25	70	°C

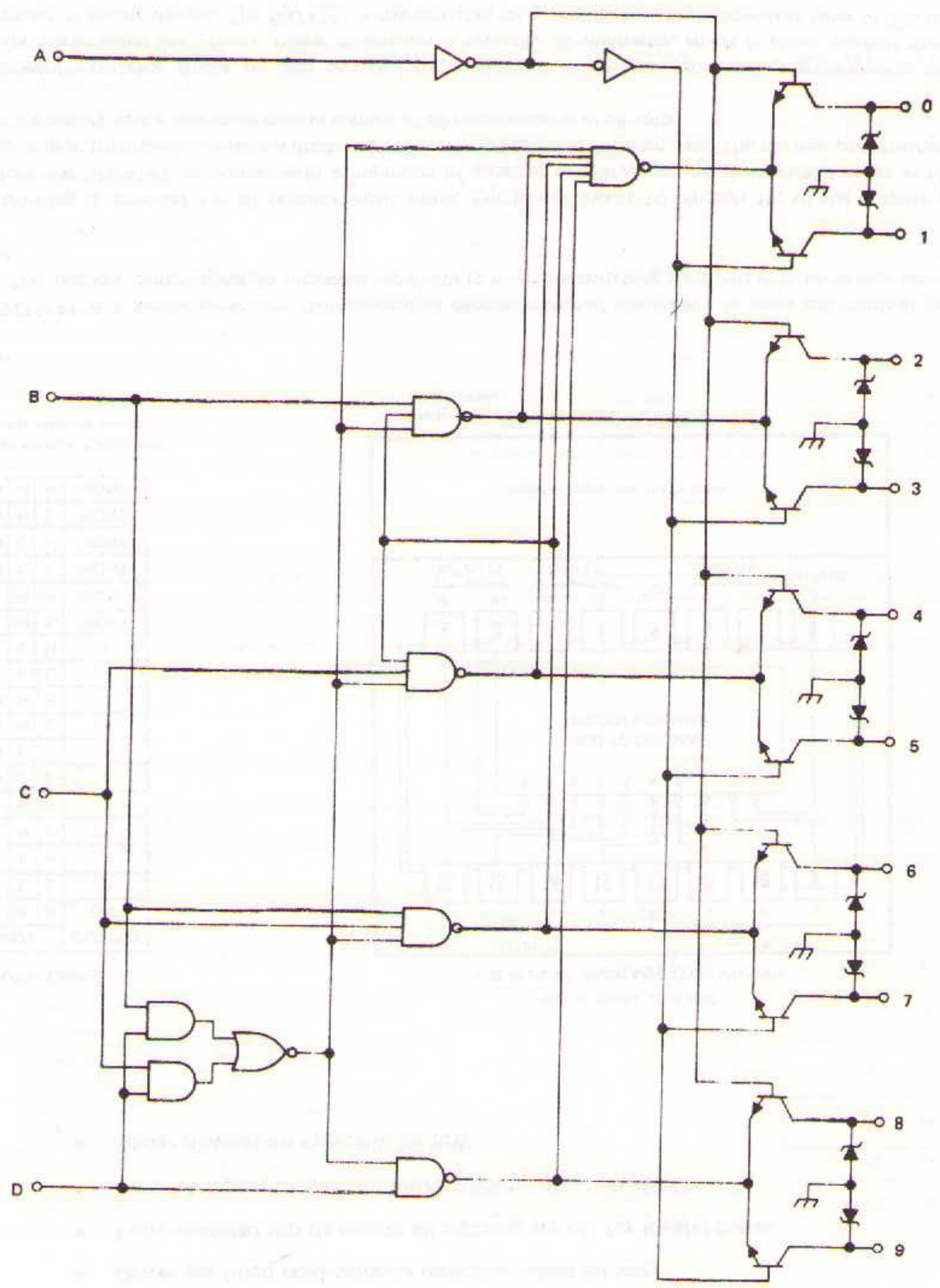
NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2		2			V
V_{IL}	Low-level input voltage	1 and 2				0.8	V
$V_{O(on)}$	On-state output voltage	1	V_{CC} = MIN, I_O = 7 mA			2.5	V
$V_{O(off)}$	Off-state output voltage for input counts 0 thru 9	2	V_{CC} = MAX, I_O = 0.5 mA	60			V
$I_{O(off)}$	Off-state reverse current	2	V_{CC} = MAX, V_O = 55 V			50	μA
$I_{O(off)}$	Off-state reverse current for input counts 10 thru 15	2	V_{CC} = MAX, V_O = 30 V			5	μA
I_{IH}	High-level input current at A	3	V_{CC} = MAX, V_I = 2.4 V			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IH}	High-level input current at B, C, or D	3	V_{CC} = MAX, V_I = 2.4 V			80	μA
			V_{CC} = MAX, V_I = 5.5 V			1	mA
I_{IL}	Low-level input current into A	4	V_{CC} = MAX, V_I = 0.4 V			−1.6	mA
I_{IL}	Low-level input current into B, C, or D					−3.2	mA
I_{CC}	Supply current	3	V_{CC} = MAX		16	25	mA

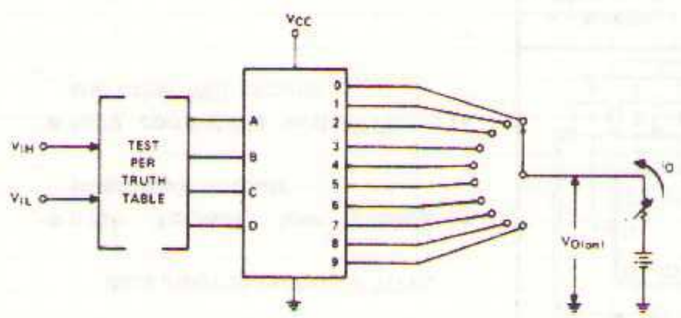
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡This typical value is at V_{CC} = 5 V, T_A = 25°C.

functional block diagram



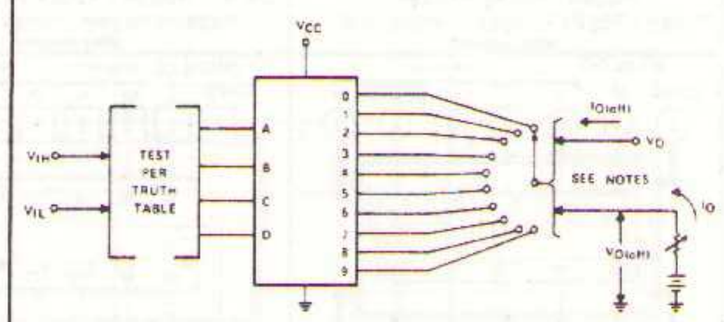
PARAMETER MEASUREMENT INFORMATION

d-c test circuits§



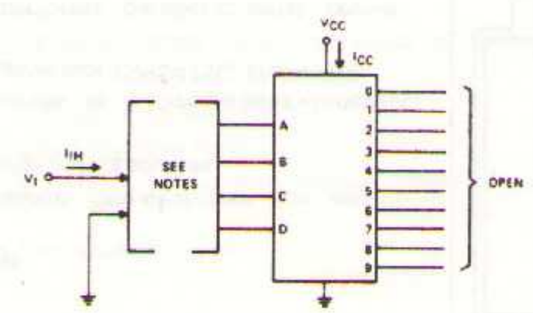
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, $V_{O(on)}$



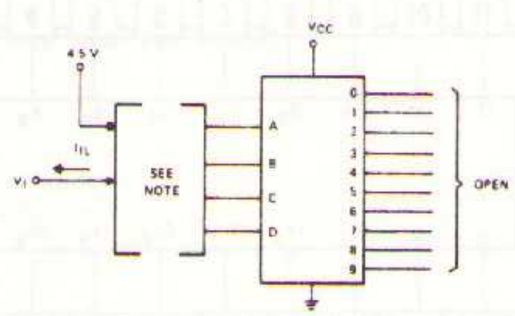
A. Each output is tested separately.
B. $V_{O(off)}$ is tested at I_O = 0.5 mA and $I_{O(off)}$ is tested at V_O = 55 V for all input counts. $I_{O(off)}$ is tested also at V_O = 30 V for input counts 10 through 15.

FIGURE 2–V_{IH}, V_{IL}, $I_{O(off)}$, $V_{O(off)}$



A. When testing I_{IH}, each input is tested separately with all other inputs grounded.
B. When testing I_{CC}, all inputs are grounded.

FIGURE 3–I_{IH}, I_{CC}



Each input is tested separately, with all other inputs at 4.5 V.

FIGURE 4–I_{IL}

§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

TYPICAL APPLICATION DATA

general

When these decoder/drivers are used in close proximity (on the same circuit board) with standard digital integrated circuits, care should be exercised to ensure that the impedance of the ground bus (including interconnections) is sufficiently low to absorb the normal energy levels resulting from switching the tube elements.

driving indicator tubes

As shown in figure A, the SN74141 requires no external components for driving cold-cathode indicator tubes. The versatility here is limited only by the system capability to control the data inputs.

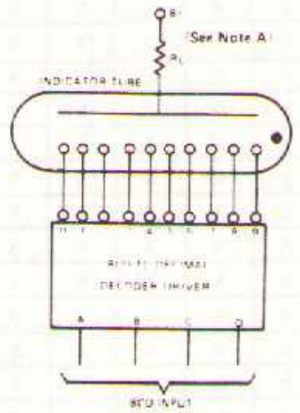


FIGURE A

A suggested method for blanking extraneous zeros is shown in figure B. Any input count above decimal 9 may be used for blanking. In the following application decimal 12 is used. When the most-significant bit (MSB) or the least-significant bit (LSB) is decimal 0(0000), that indicator is blanked while decimal 12 (binary 1100) is applied to the SN74141 inputs causing all the outputs to be off. If the MSB or LSB is decimal 0 and being blanked, this signal is gated with and blanks the next smaller digit. This scheme is easily expandable to n-digits.

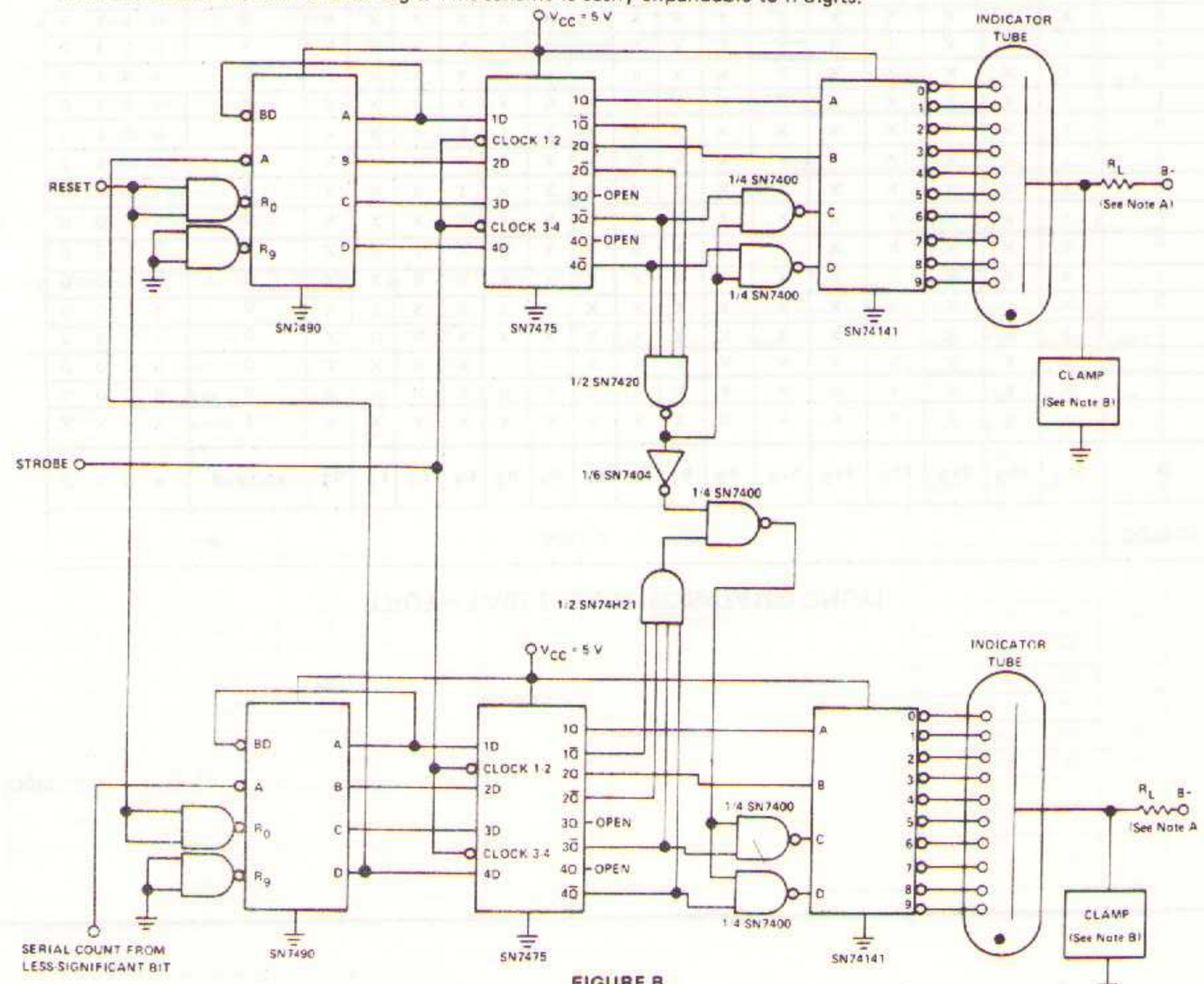


FIGURE B

NOTES: A. Values for B+ and R_L are as specified by the tube manufacturer.
B. Blanking is assured only if the anode of the indicator tube is clamped at 150 volts maximum.

features

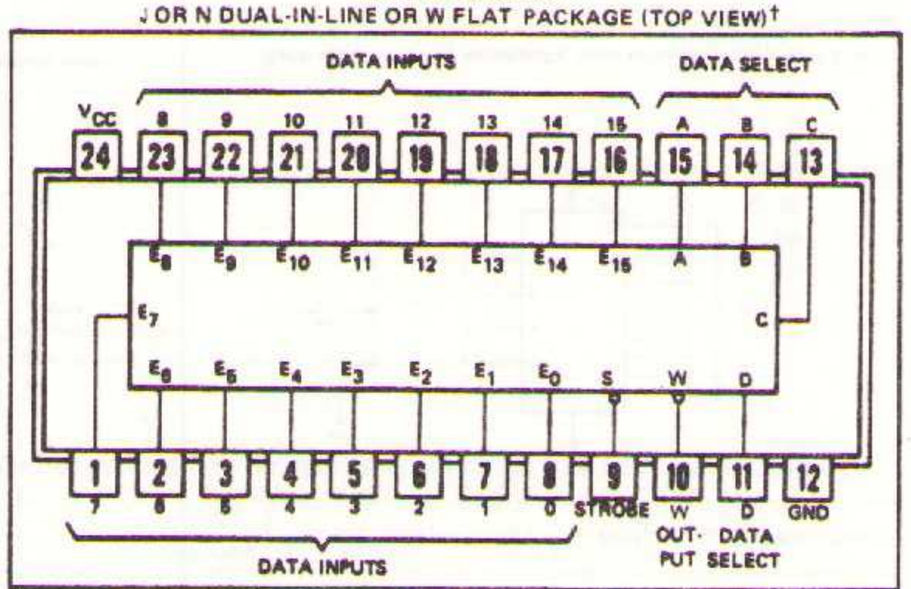
- selects one-of-sixteen (or one-of-eight) data sources
- serves as a five-variable-function generator (SN54150, SN74150)
- performs parallel-to-serial conversion
- permits multiplexing from N lines to 1 line
- input-clamping diodes simplify system design
- typical propagation delay times:

  through 4 select levels – 28 ns

  through 3 select levels – 20 ns

  data input to output – 10 ns
- high fan-out, low impedance, totem-pole outputs
- fully compatible with TTL, DTL and other MSI circuits

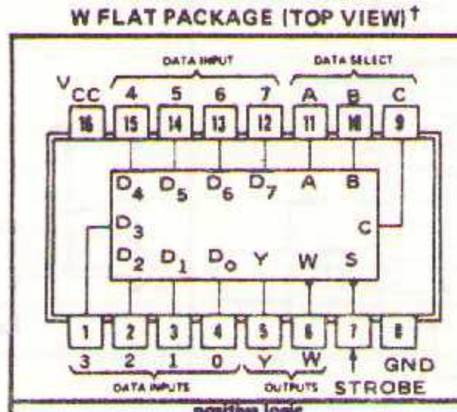
SN54150, SN74150
J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic

$$W = S(\bar{A}\bar{B}\bar{C}\bar{D}E_0 + A\bar{B}\bar{C}\bar{D}E_1 + \bar{A}B\bar{C}\bar{D}E_2 + AB\bar{C}\bar{D}E_3 + \bar{A}\bar{B}C\bar{D}E_4 + A\bar{B}C\bar{D}E_5 + \bar{A}BC\bar{D}E_6 + ABC\bar{D}E_7$$
$$\bar{A}\bar{B}\bar{C}DE_8 + A\bar{B}\bar{C}DE_9 + \bar{A}B\bar{C}DE_{10} + AB\bar{C}DE_{11} + \bar{A}\bar{B}CDE_{12} + A\bar{B}CDE_{13} + \bar{A}BCDE_{14} + ABCDE_{15})$$

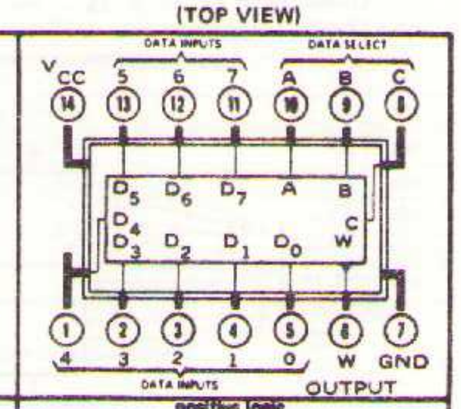
SN54151, SN74151
J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



positive logic

$$Y = S(\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + \bar{A}B\bar{C}D_2 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7) \quad W = \bar{Y}$$

SN54152, SN74152
W FLAT PACKAGE
(TOP VIEW)



positive logic

$$W = (\bar{A}\bar{B}\bar{C}D_0 + A\bar{B}\bar{C}D_1 + AB\bar{C}D_3 + \bar{A}\bar{B}CD_4 + A\bar{B}CD_5 + \bar{A}BCD_6 + ABCD_7)$$

†Pin assignments for these circuits are the same for all packages.

description

Each of these monolithic, data selectors/multiplexers contain inverter/drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-INVERT gate. The SN54151/74151 features complementary outputs whereas the SN54150/SN74150 and SN54152/SN74152 have inverted outputs only. The SN54150/SN74150 and SN54151/SN74151 circuits are provided with a strobe-input which, when taken to a logical 0, enables the function of these multiplexers.

These data selectors/multiplexers are fully compatible for use with other TTL or DTL circuits. Each input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized Series 54/74 loads is provided in the logical 1 state to facilitate connection of unused inputs to used inputs. Typical power dissipations are:

SN54150/SN74150 – 200 milliwatts
SN54151/SN74151 – 145 milliwatts
SN54152/SN74152 – 130 milliwatts

These data selectors feature Series 54H/74H circuitry for the OR function. This is done to minimize the capacitive effects of paralleling the phase-splitter transistors and thus reduce the propagation delay time. The SN54150, SN54151, and SN54152 are characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74150, SN74151 and SN74152 are characterized for operation from 0°C to 70°C.

logic

TRUTH TABLE (SN54150/SN74150 ONLY)

INPUTS																		OUTPUT
D	C	B	A	STROBE	E_0	E_1	E_2	E_3	E_4	E_5	E_6	E_7	E_8	E_9	E_{10}	E_{11}	E_{12}	E_{13}	E_{14}	E_{15}	W
X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	0	0	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	0	1	0	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	0	1	0	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	0	0	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	0	0	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	X	0
0	0	1	1	0	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	X	1
0	0	1	1	0	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	0	0	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	X	1
0	1	0	0	0	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	X	0
0	1	0	1	0	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	X	1
0	1	0	1	0	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	X	0
0	1	1	0	0	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	X	1
0	1	1	0	0	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	X	0
0	1	1	1	0	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	X	1
0	1	1	1	0	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	X	0
1	0	0	0	0	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	X	1
1	0	0	0	0	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	X	0
1	0	0	1	0	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	X	1
1	0	0	1	0	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	X	0
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	X	1
1	0	1	0	0	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	X	0
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	X	1
1	0	1	1	0	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	X	0
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	X	1
1	1	0	0	0	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	X	0
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	X	1
1	1	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	X	0
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	X	1
1	1	1	0	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	X	0
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1
1	1	1	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0

When used to indicate an input condition, X = LOGICAL 1 OR LOGICAL 0

logic (continued)

TRUTH TABLE (SN54151/SN74151 AND SN54152/SN74152 ONLY)

INPUTS												OUTPUTS	
C	B	A	STROBE(1)	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7	Y(1)	W
X	X	X	1	X	X	X	X	X	X	X	X	0	1
0	0	0	0	0	X	X	X	X	X	X	X	0	1
0	0	0	0	1	X	X	X	X	X	X	X	1	0
0	0	1	0	X	0	X	X	X	X	X	X	0	1
0	0	1	0	X	1	X	X	X	X	X	X	1	0
0	1	0	0	X	X	0	X	X	X	X	X	0	1
0	1	0	0	X	X	1	X	X	X	X	X	1	0
0	1	1	0	X	X	X	0	X	X	X	X	0	1
0	1	1	0	X	X	X	1	X	X	X	X	1	0
1	0	0	0	X	X	X	X	0	X	X	X	0	1
1	0	0	0	X	X	X	X	1	X	X	X	1	0
1	0	1	0	X	X	X	X	X	0	X	X	0	1
1	0	1	0	X	X	X	X	X	1	X	X	1	0
1	1	0	0	X	X	X	X	X	X	0	X	0	1
1	1	0	0	X	X	X	X	X	X	1	X	1	0
1	1	1	0	X	X	X	X	X	X	X	0	0	1
1	1	1	0	X	X	X	X	X	X	X	1	1	0

NOTES: 1. SN54151/SN74151 only.
2. When used to indicate an input, X = irrelevant.

absolute maximum ratings (over operating temperature range unless otherwise noted)

Supply Voltage V_{CC} (See Note 1) . . . . . 7 V
Input Voltage, V_{in} (See Note 1) . . . . . 5.5 V
Operating Free-Air Temperature Range: SN54150, SN54151, SN54152 Circuits . . . . . −55°C to 125°C
SN74150, SN74151, SN74152 Circuits . . . . . 0°C to 70°C
Storage Temperature Range . . . . . −65°C to 150°C

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1): SN54150, SN54151, SN54152 Circuits	4.5	5	5.5	V
SN74150, SN74151, SN74152 Circuits	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N): Logical 0			10	
Logical 1			20	

electrical characteristics over recommended operating temperature range (unless otherwise noted)

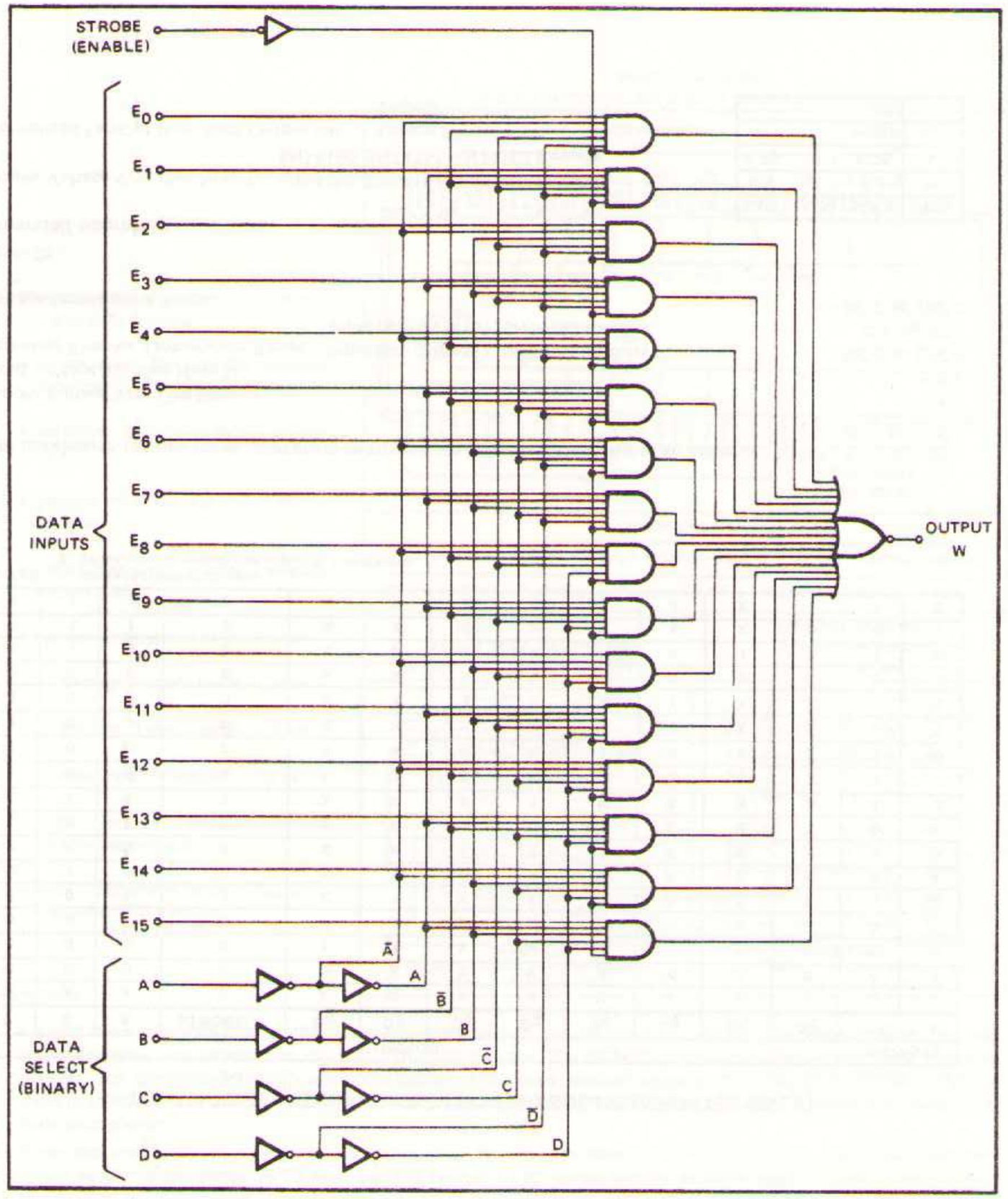
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	2					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1 AND 2	V_{CC} = MIN, I_{load} = −800 μA	$V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V,	2.4			V
$V_{out(0)}$	Logical 0 output voltage	1 AND 2	V_{CC} = MIN, I_{sink} = 16 mA	$V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V,			0.4	V
$I_{in(1)}$	Logical 1 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 2.4 V			40	μA
			V_{CC} = MAX,	V_{in} = 5.5 V			1	mA
$I_{in(0)}$	Logical 0 level input current (each input)	3	V_{CC} = MAX,	V_{in} = 0.4 V			−1.6	mA
I_{OS}	Short circuit output current §	4	V_{CC} = MAX, V_{out} = 0	SN54150, SN54151, SN54152	−20		−55	mA
				SN74150, SN74151, SN74152	−18		−55	mA
I_{CC}	Supply current (SN54150/SN74150)	5	V_{CC} = MAX,	V_{in} = 4.5 V		40	68	mA
I_{CC}	Supply current (SN54151/SN74151)	5	V_{CC} = MAX,	V_{in} = 4.5 V		29	48	mA
I_{CC}	Supply current (SN54152/SN74152)	5	V_{CC} = MAX,	V_{in} = 4.5 V		26	43	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

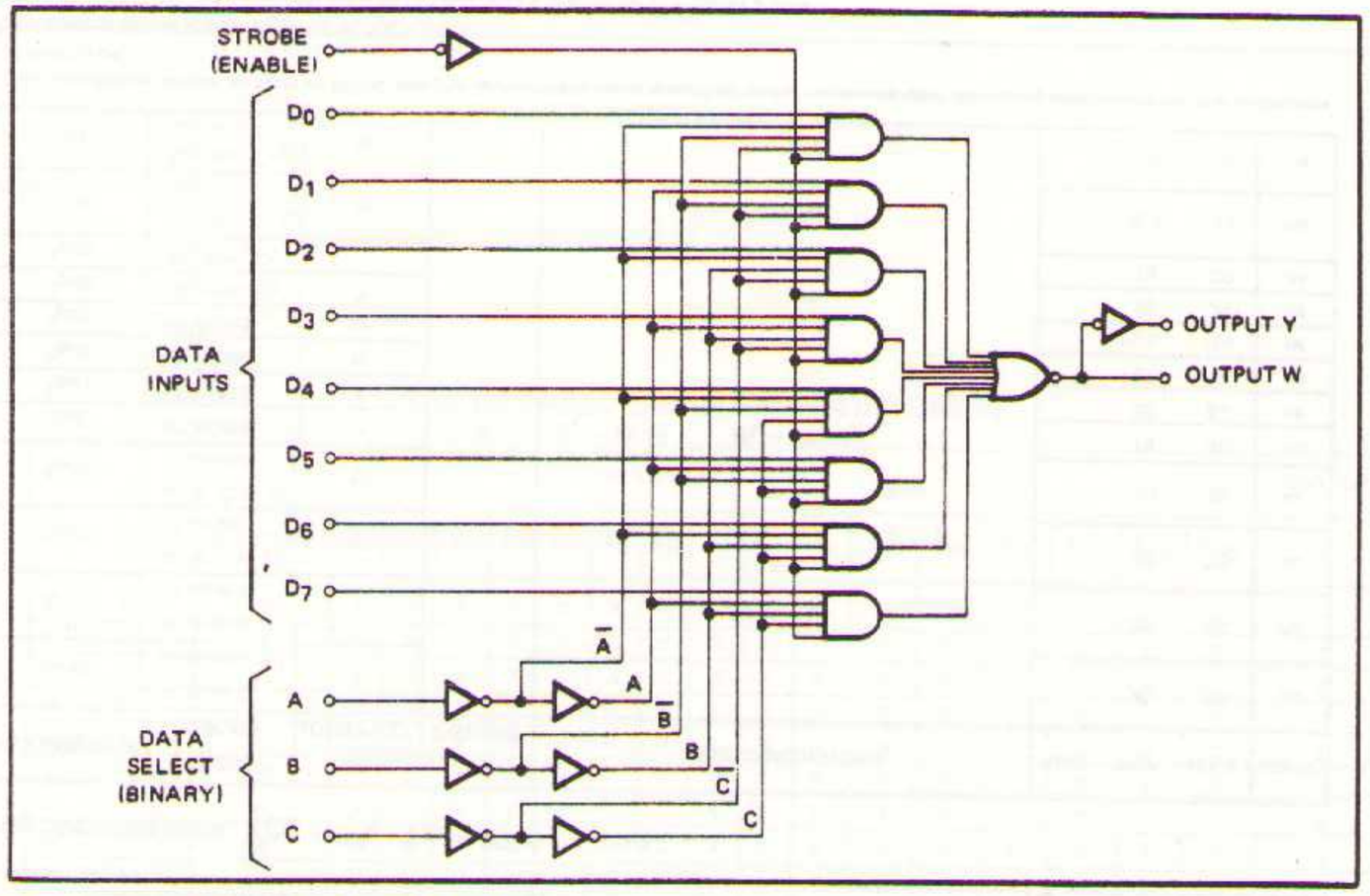
PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd0}	A, B, or C (4 levels)	Y	6	C_L = 15 pF R_L = 400 Ω		20	30	ns
t_{pd1}	A, B, or C (4 levels)	Y				35	52	ns
t_{pd0}	A, B, C, or D (3 levels)	W				22	33	ns
t_{pd1}	A, B, C, or D (3 levels)	W				23	35	ns
t_{pd0}	STROBE	Y				19	30	ns
t_{pd1}	STROBE	Y				35	52	ns
t_{pd0}	STROBE	W				21	30	ns
t_{pd1}	STROBE	W				15.5	24	ns
t_{pd0}	D_0 thru D_7	Y				16	24	ns
t_{pd1}	D_0 thru D_7	Y				19	29	ns
t_{pd0}	E_0 thru E_{15}, D_0 thru D_7	W				8.5	14	ns
t_{pd1}	E_0 thru E_{15}, D_0 thru D_7	W				13	20	ns

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable circuit type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output of the SN54151/SN74151 should be shorted at a time.

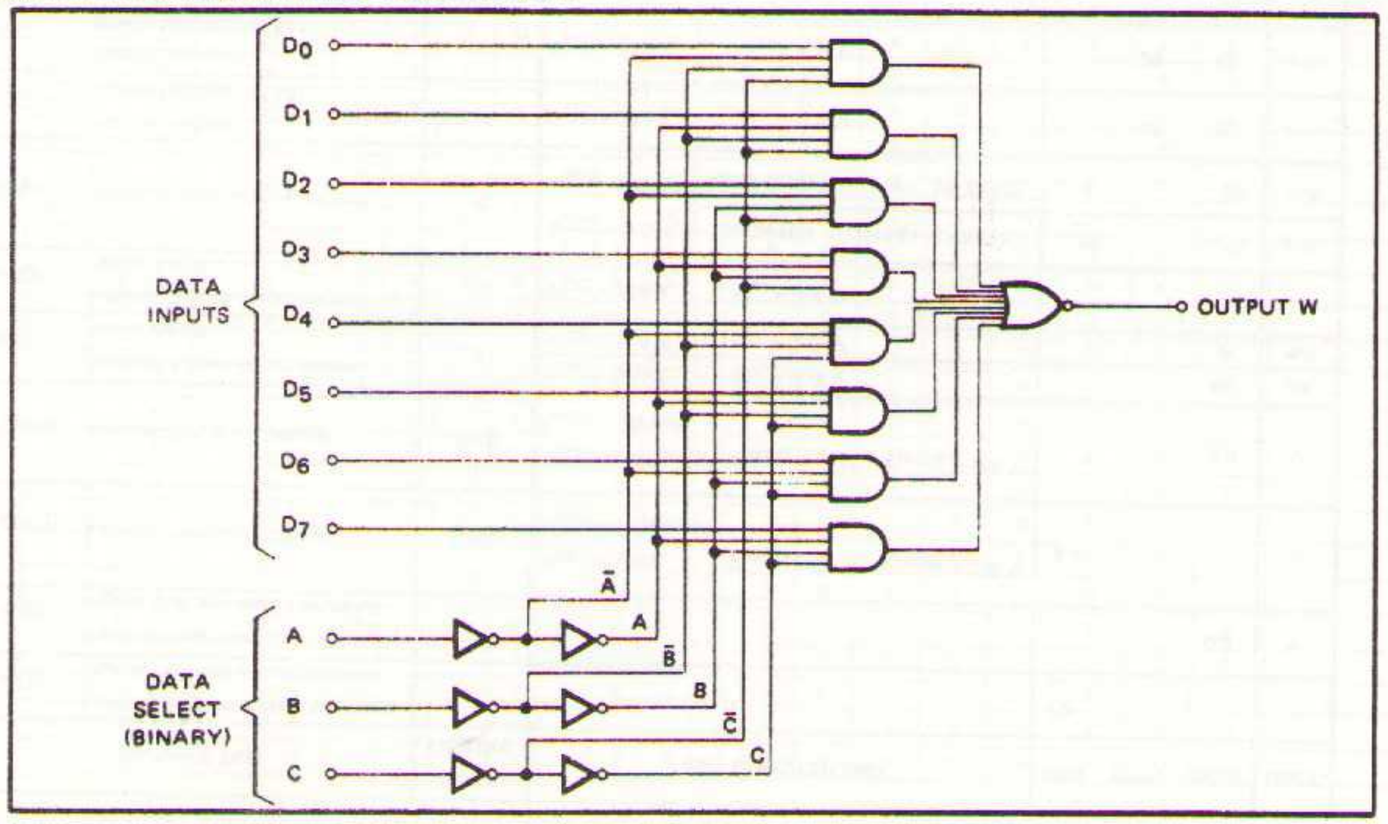
functional block diagram



functional block diagram (SN54151, SN74151)

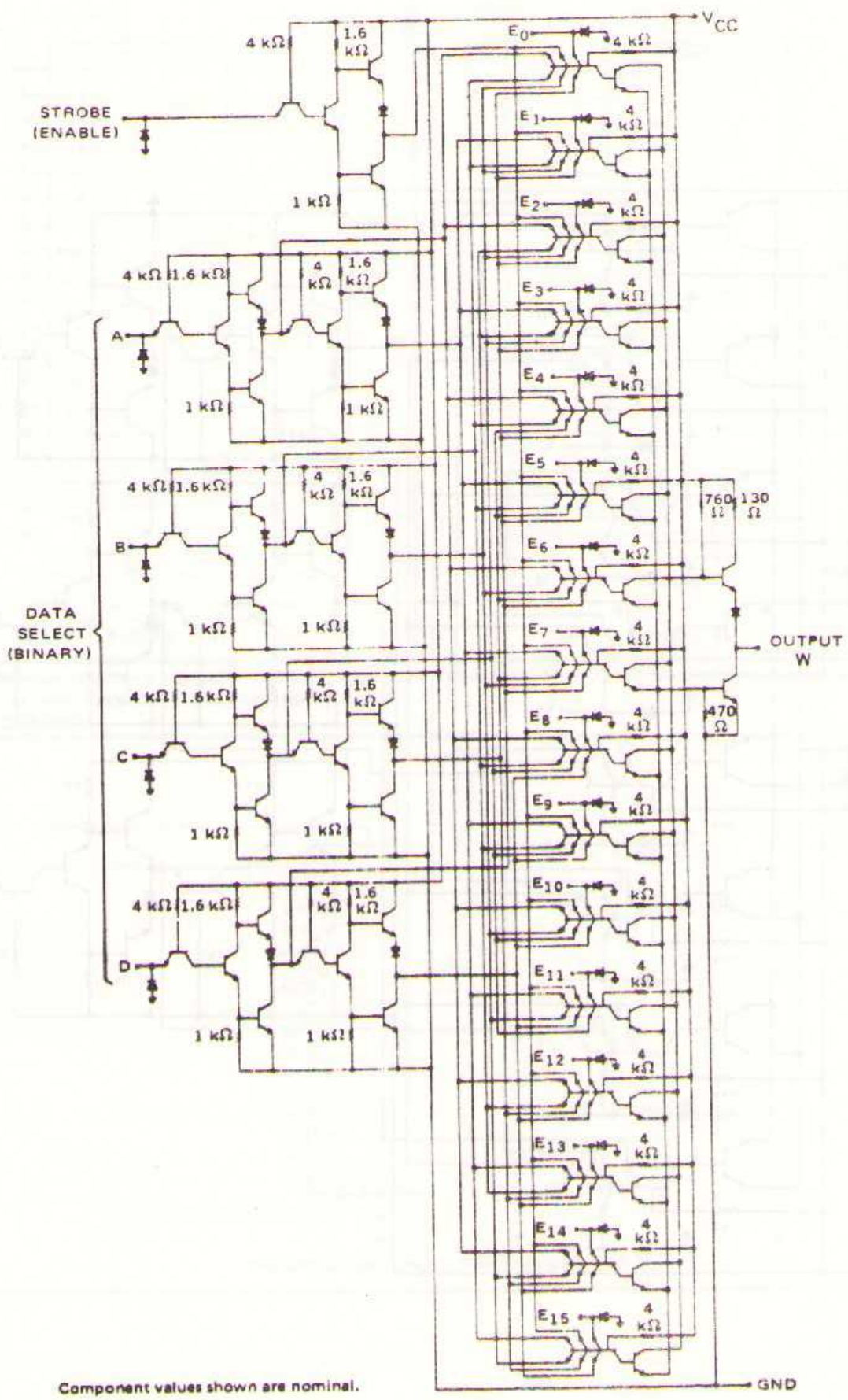


functional block diagram (SN54152, SN74152)



SN 74150 N

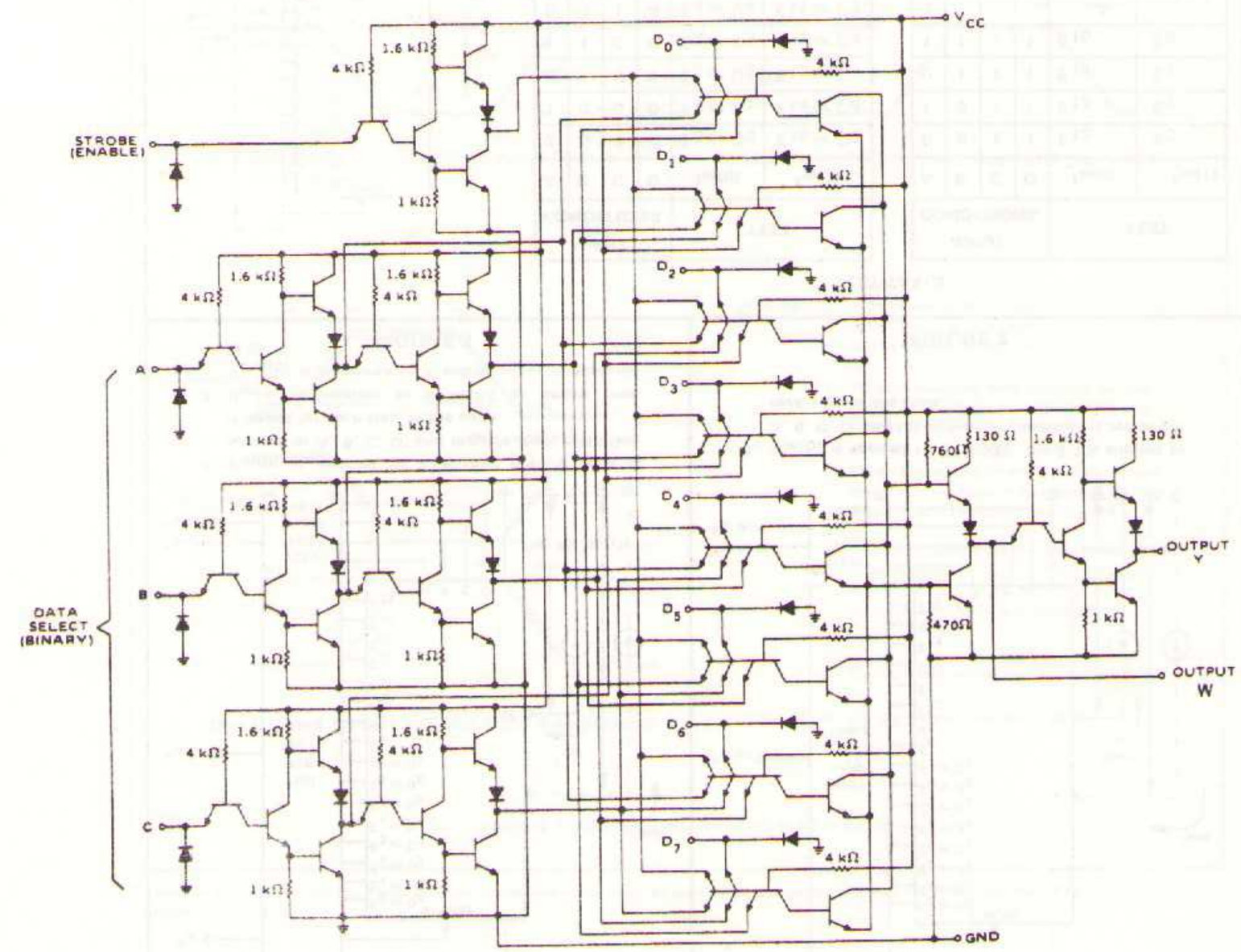
schematic



Component values shown are nominal.

SN 74151 N

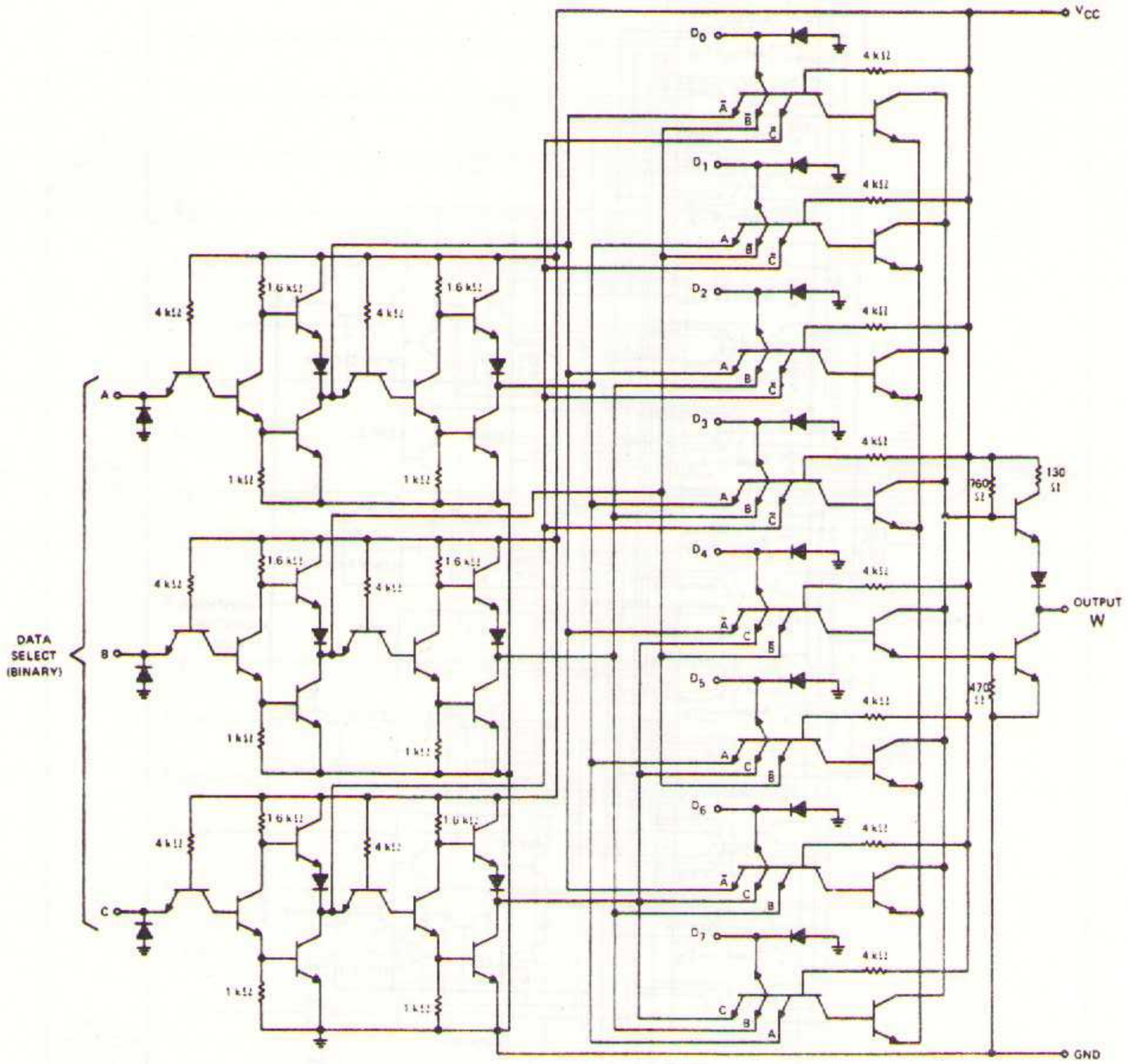
schematic



Component values shown are nominal.

SN 74152

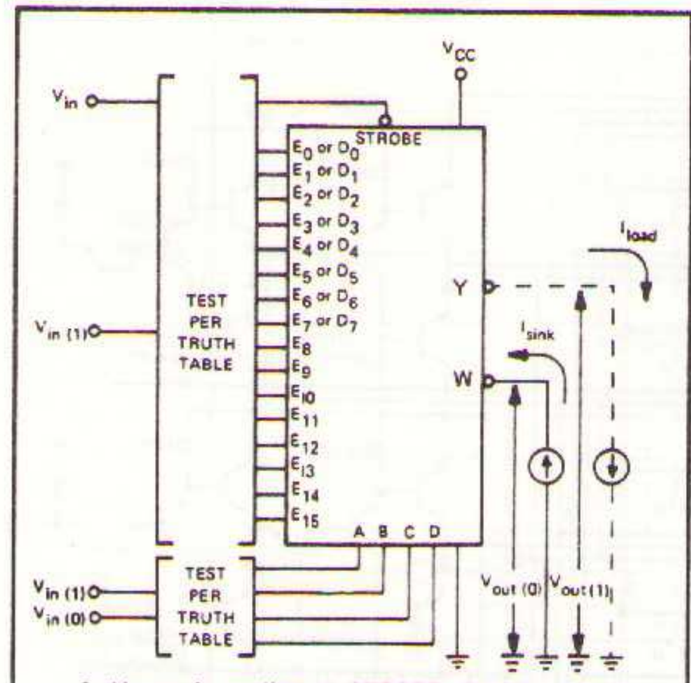
schematic



Component values shown are nominal.

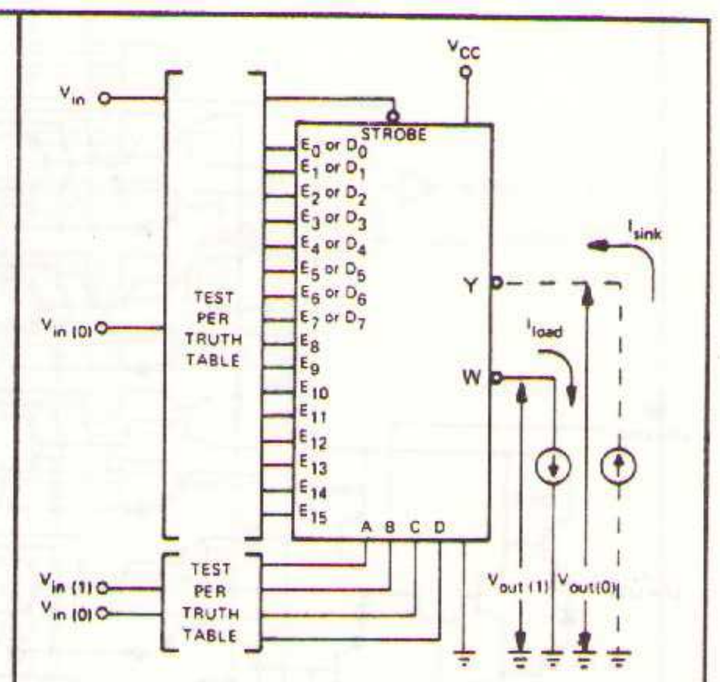
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 code is applied to A, B, C, D; and input/output condition is tested for each step of the code.
2. $V_{in(1)}$ is applied to STROBE at which time $V_{out(0)}$ is measured at Y and $V_{out(1)}$ is measured at W.

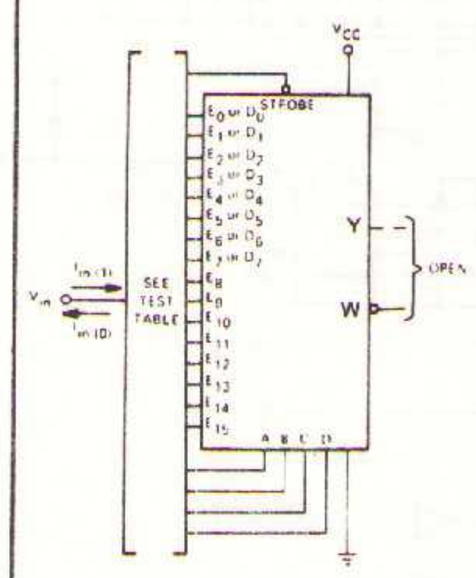
FIGURE 1



1. $V_{in(0)}$ is applied to STROBE; 8-4-2-1 is applied to A, B, C, D; and input/output condition is tested for each step of the code.

FIGURE 2

TEST TABLE



INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	0	0	E_0 or D_0	E_{15} or D_7
1	0	0	0	E_1 or D_1	E_{14} or D_6
0	1	0	0	E_2 or D_2	E_{13} or D_5
1	1	0	0	E_3 or D_3	E_{12} or D_4
0	0	1	0	E_4 or D_4	E_{11} or D_3
1	0	1	0	E_5 or D_5	E_{10} or D_2
0	1	1	0	E_6 or D_6	E_9 or D_1
1	1	1	0	E_7 or D_7	E_8 or D_0
0	0	0	1	E_8	E_7
1	0	0	1	E_9	E_6
0	1	0	1	E_{10}	E_5
1	1	0	1	E_{11}	E_4

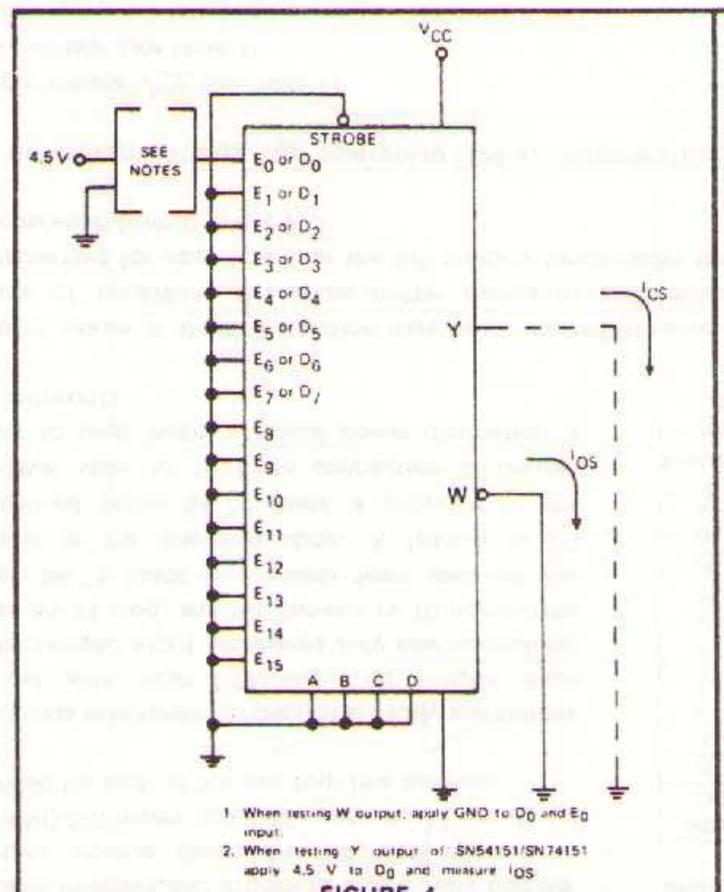
INPUT CONDITIONS				TEST	
A	B	C	D	$I_{in(0)}$	$I_{in(1)}$
0	0	1	1	E_{12}	E_3
1	0	1	1	E_{13}	E_2
0	1	1	1	E_{14}	E_1
1	1	1	1	E_{15}	E_0
0				A	
	0			B	
		0		C	
			0	D	
1					A
	1				B
		1			C
			1		D

1. When testing strobe input, all other inputs are open.

FIGURE 3

† Arrows indicate actual direction of current flow. Tests as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

d-c test circuits† (continued)



1. When testing W output, apply GND to D_0 and E_0 input.
2. When testing Y output of SN54151/SN74151 apply 4.5 V to D_0 and measure I_{OS}.

FIGURE 4

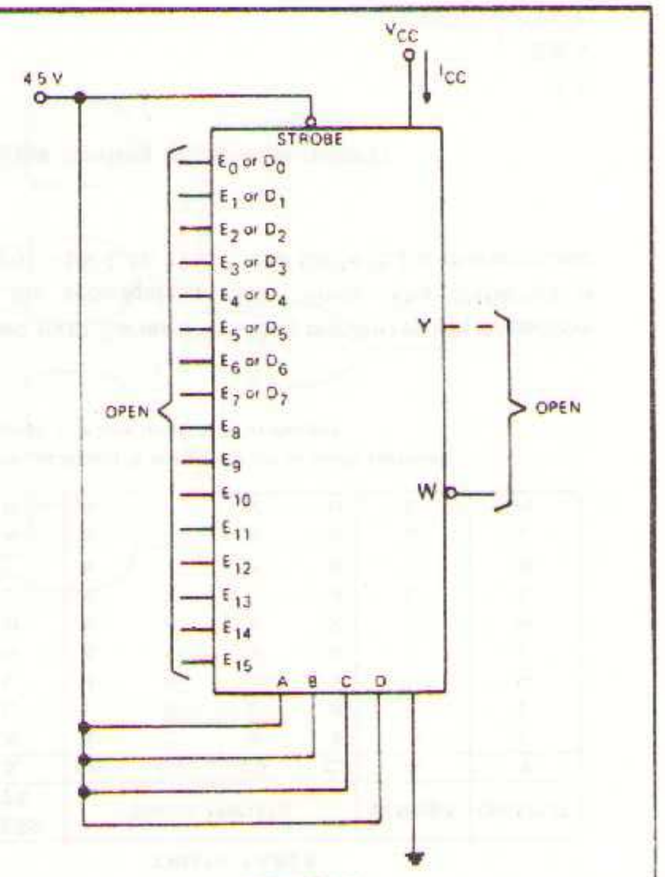


FIGURE 5

† Arrows indicate actual direction of current flow. Tests, as shown are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

switching characteristics†

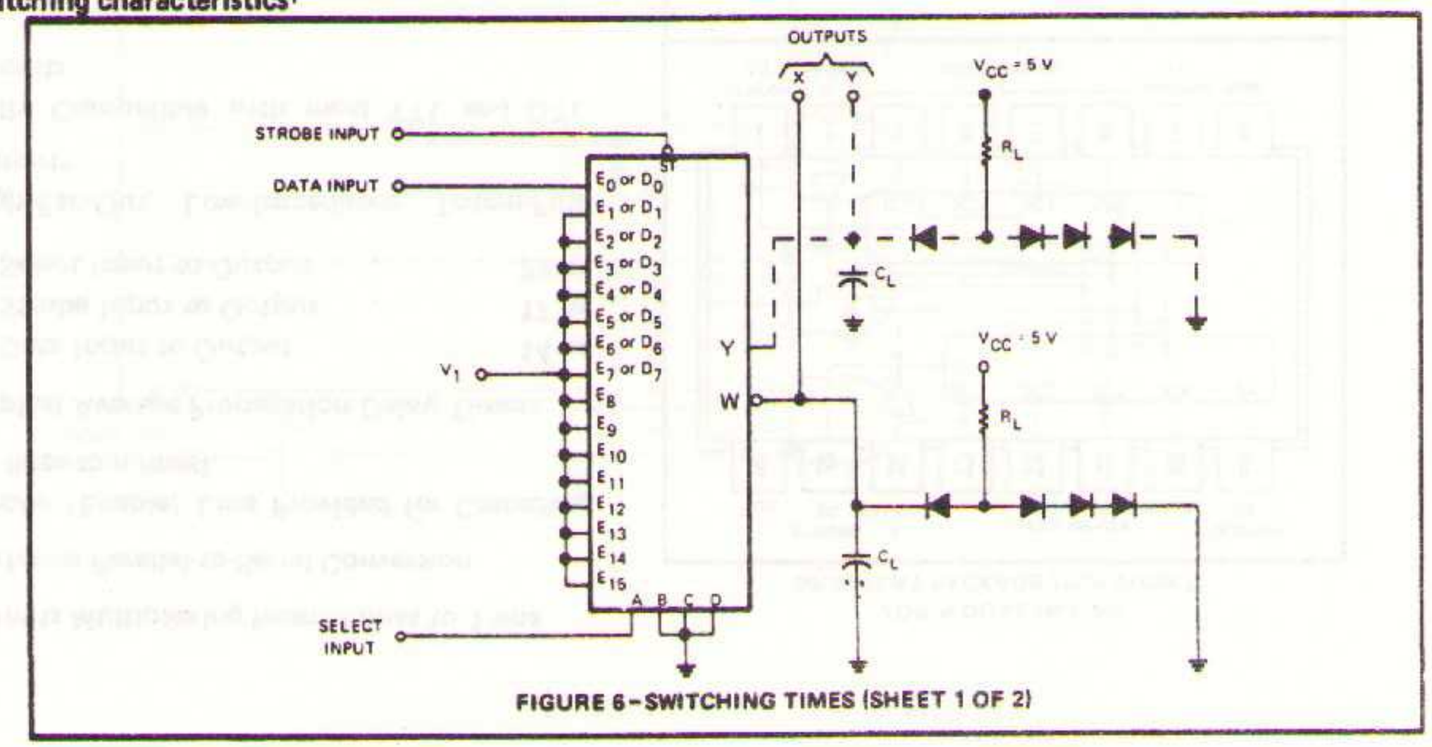
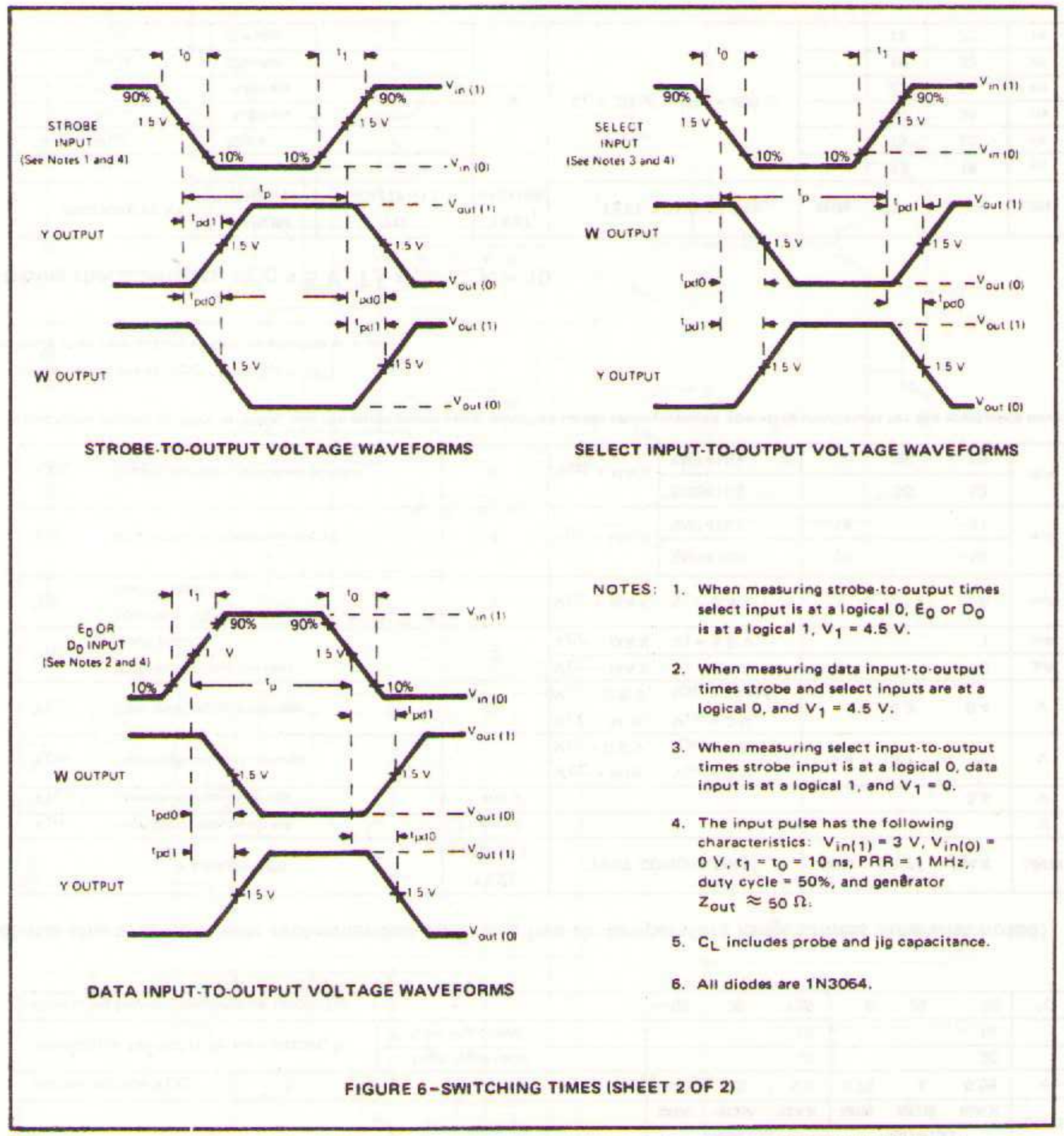


FIGURE 6–SWITCHING TIMES (SHEET 1 OF 2)

switching characteristics (continued)



STROBE-TO-OUTPUT VOLTAGE WAVEFORMS

SELECT INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

DATA INPUT-TO-OUTPUT VOLTAGE WAVEFORMS

NOTES:
1. When measuring strobe-to-output times select input is at a logical 0, E_0 or D_0 is at a logical 1, V_1 = 4.5 V.
2. When measuring data input-to-output times strobe and select inputs are at a logical 0, and V_1 = 4.5 V.
3. When measuring select input-to-output times strobe input is at a logical 0, data input is at a logical 1, and V_1 = 0.
4. The input pulse has the following characteristics: $V_{in(1)}$ = 3 V, $V_{in(0)}$ = 0 V, $t_1 = t_0$ = 10 ns, PRR = 1 MHz, duty cycle = 50%, and generator $Z_{out} \approx 50\ \Omega$.
5. C_L includes probe and jig capacitance.
6. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES (SHEET 2 OF 2)

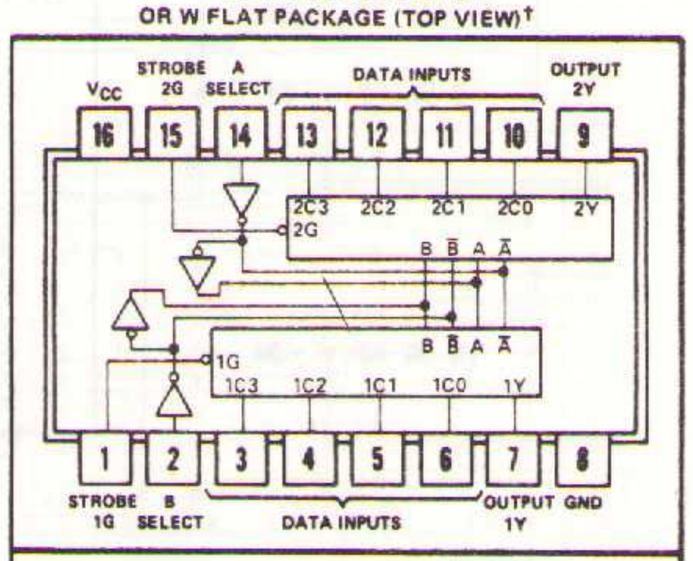
† Tests, as shown, are for the SN54150/SN74150. Identical tests as applicable are performed for the SN54151/SN74151 and SN54152/SN74152.

- **Permits Multiplexing from N lines to 1 line**
- **Performs Parallel-to-Serial Conversion**
- **Strobe (Enable) Line Provided for Cascading (N lines to n lines)**
- **Typical Average Propagation Delay Times:**

  Data Input to Output . . . . . 14 ns
  Strobe Input to Output . . . . 17 ns
  Select Input to Output . . . . . 22 ns

- **High-Fan-Out, Low-Impedance, Totem-Pole Outputs**
- **Fully Compatible with most TTL and DTL Circuits**

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

†Pin assigments for these circuits are the same for all packages.

TRUTH TABLE

ADDRESS INPUTS		DATA INPUTS				STROBE	OUTPUT
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

Address inputs A and B are common to both sections.
H = high level, L = low level, X = irrelevant

description

Each of these monolithic, data selectors/multiplexers contains inverters and drivers to supply fully complementary, on-chip, binary decoding data selection to the AND-OR-invert gates. Separate strobe inputs are provided for each of the two four-line sections.

These data selectors/multiplexers are fully compatible for use with most TTL and DTL circuits. Each diode-clamped input represents only one normalized Series 54/74 load, and full fan-out to 10 normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Typical power dissipation is 180 milliwatts.

Resistor values in the OR function have been reduced to values used with Series 54H. This minimizes the capacitive effects of paralleling the phase-splitter transistors and reduces the propagation delay times. The SN54153 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74153 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54153 Circuits . . . . . −55°C to 125°C
SN74153 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54153			SN74153			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4	3.1		V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.2	0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54153	−20		−55	mA
				SN74153	−18		−57	
I_{CCL}	Supply current, low-level output	5	V_{CC} = MAX	SN54153		36	52	mA
				SN74153		36	60	

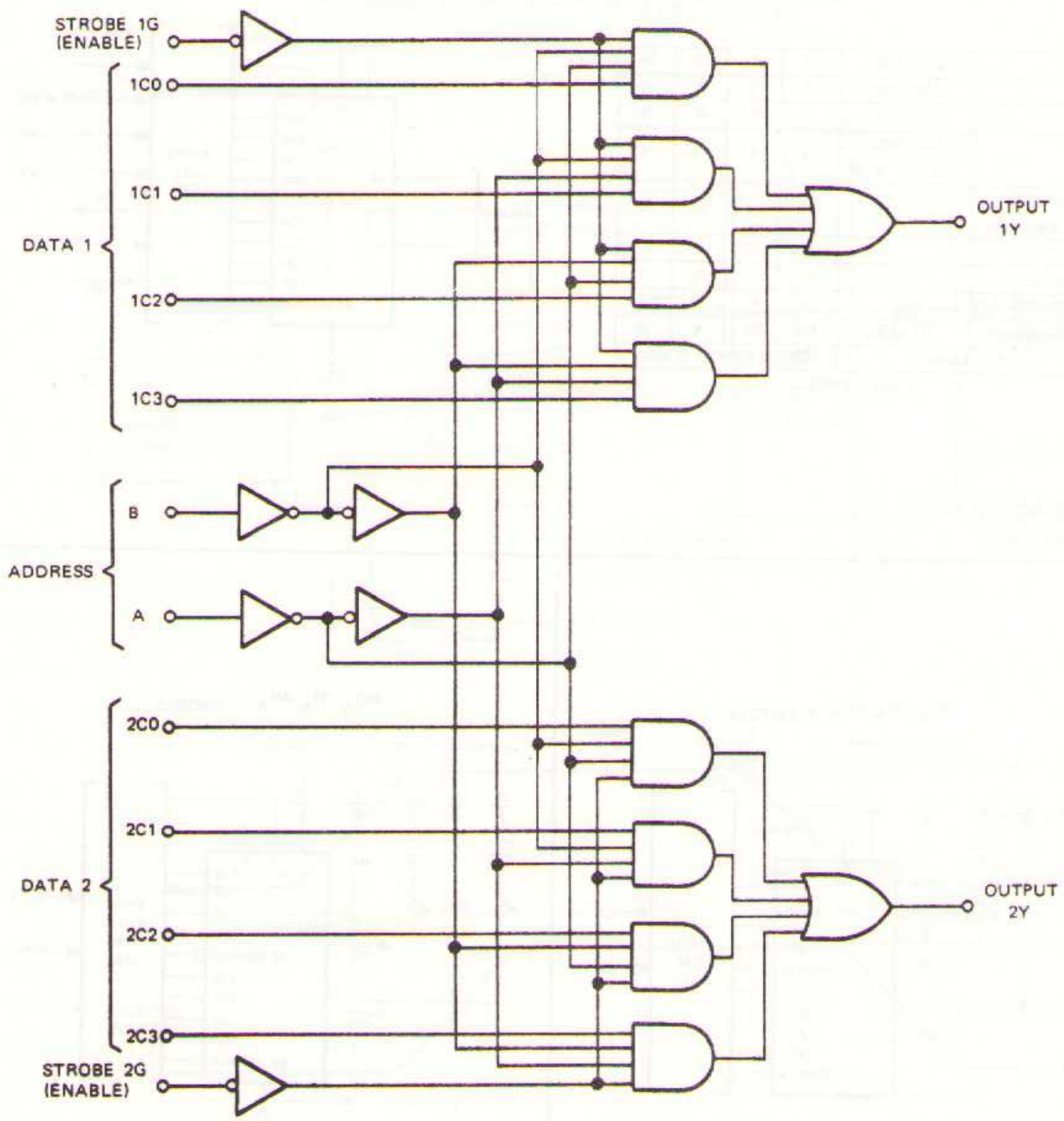
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

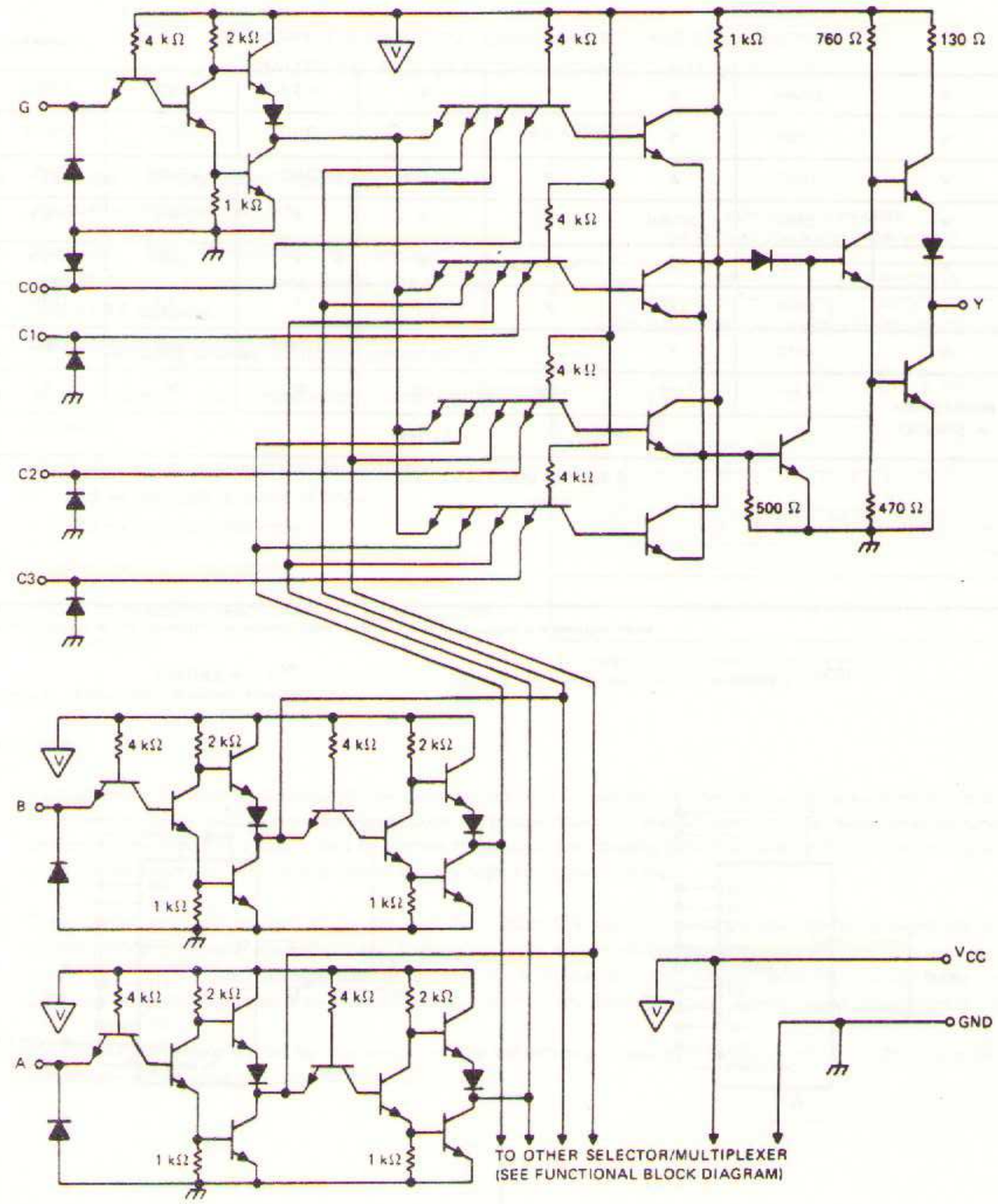
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Data	Y	6	C_L = 30 pF, R_L = 400 Ω		12	18	ns
t_{PHL}	Data	Y				15	23	ns
t_{PLH}	Address	Y				22	34	ns
t_{PHL}	Address	Y				22	34	ns
t_{PLH}	Strobe	Y				19	30	ns
t_{PHL}	Strobe	Y				15	23	ns

¶t_{PLH} = propagation delay time, low-to-high-level output.
t_{PHL} = propagation delay time, high-to-low-level output.

functional block diagram



schematic (each selector/multiplexer, and the common address section)



NOTE: Component values shown are nominal.

$-V_{CC}$ bus

PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

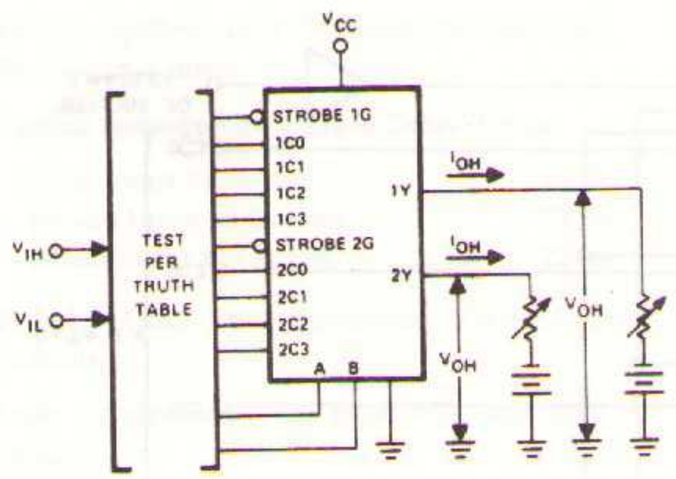


FIGURE 1–V_{IH}, V_{IL}, V_{OH}

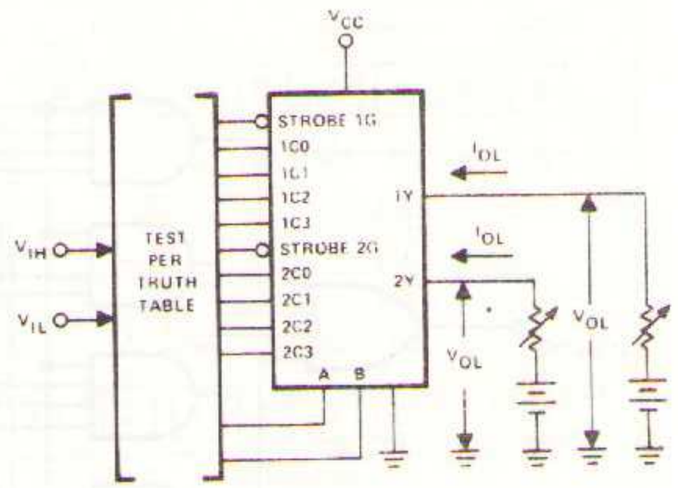
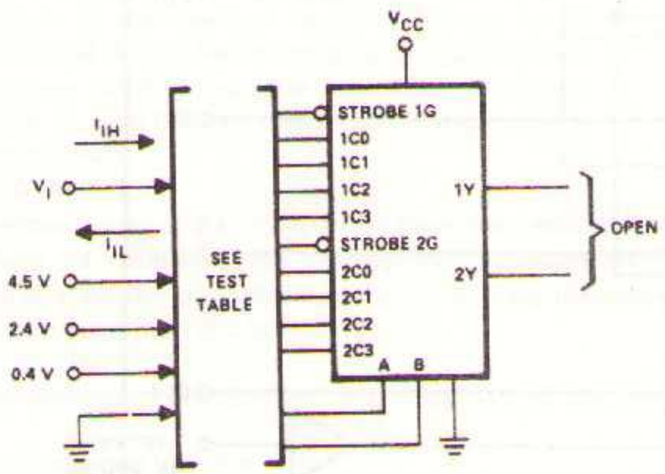


FIGURE 2–V_{IH}, V_{IL}, V_{OL}



TEST TABLE

INPUT CONDITIONS				APPLY V_I	
B	A	1G	2G	TEST I_{IL}	TEST I_{IH}
L	L	H	H		1C3, 2C3
L	H	H	H		1C2, 2C2
H	L	H	H		1C1, 2C1
H	H	H	H		A, B, 1G, 2G, 1C0, 2C0
L	L	L	L	A, B, 1G, 2G, 1C0, 2C0	
L	H	L	L	1C1, 2C1	
H	L	L	L	1C2, 2C2	
H	H	L	L	1C3, 2C3	

H = 2.4 V, L = 0.4 V

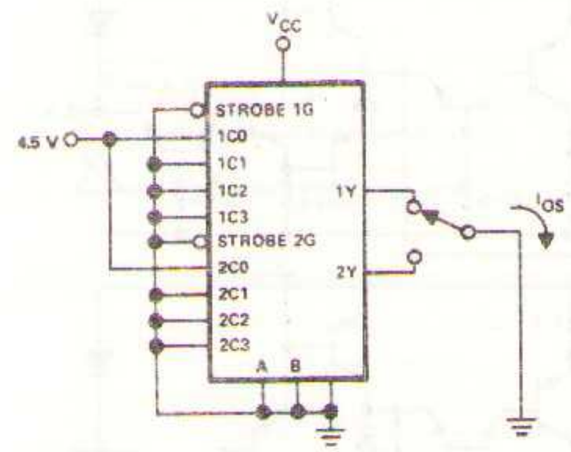
NOTE: Each input is tested separately. When I_{IH} is tested, all C inputs not under test are grounded. When I_{IL} is tested, all C inputs not under test are at 4.5 V.

FIGURE 3 –I_{IH}, I_{IL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)



NOTE: Each output is tested separately.

FIGURE 4 – I_{OS}

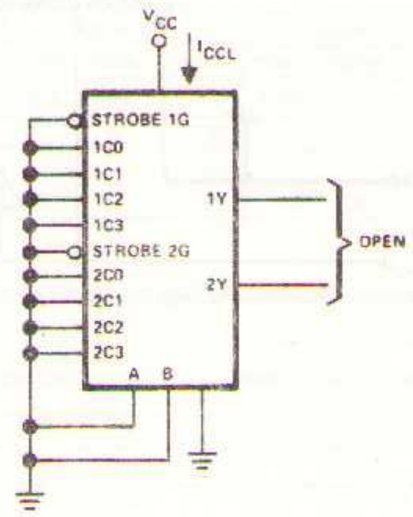


FIGURE 5 – I_{CCL}

† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

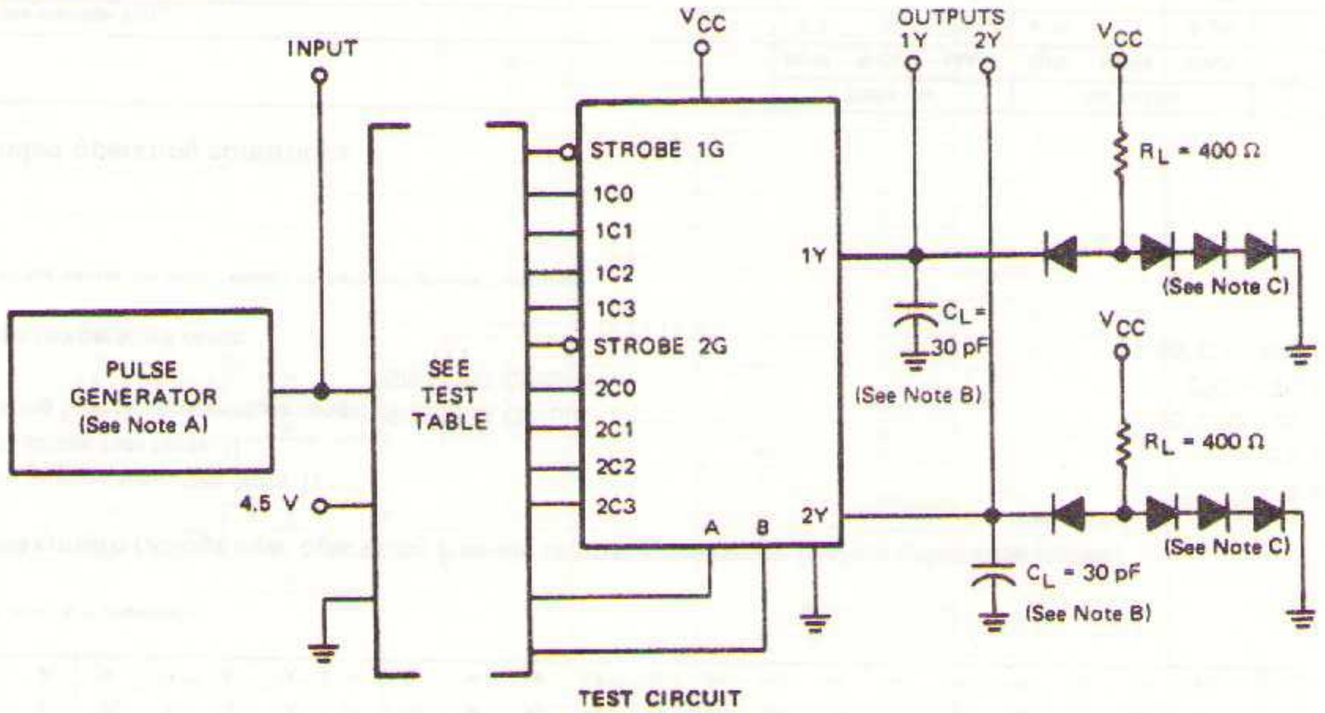
TEST TABLE FOR FIGURE 6

INPUTS							OUTPUT Y WAVEFORM
B	A	C0	C1	C2	C3	G	
GND	GND	INPUT	X	X	X	GND	A
GND	4.5 V	X	INPUT	X	X	GND	A
4.5 V	GND	X	X	INPUT	X	GND	A
4.5 V	4.5 V	X	X	X	INPUT	GND	A
GND	INPUT	GND	4.5 V	X	X	GND	A
INPUT	GND	GND	X	4.5 V	X	GND	A
GND	GND	4.5 V	X	X	X	INPUT	B

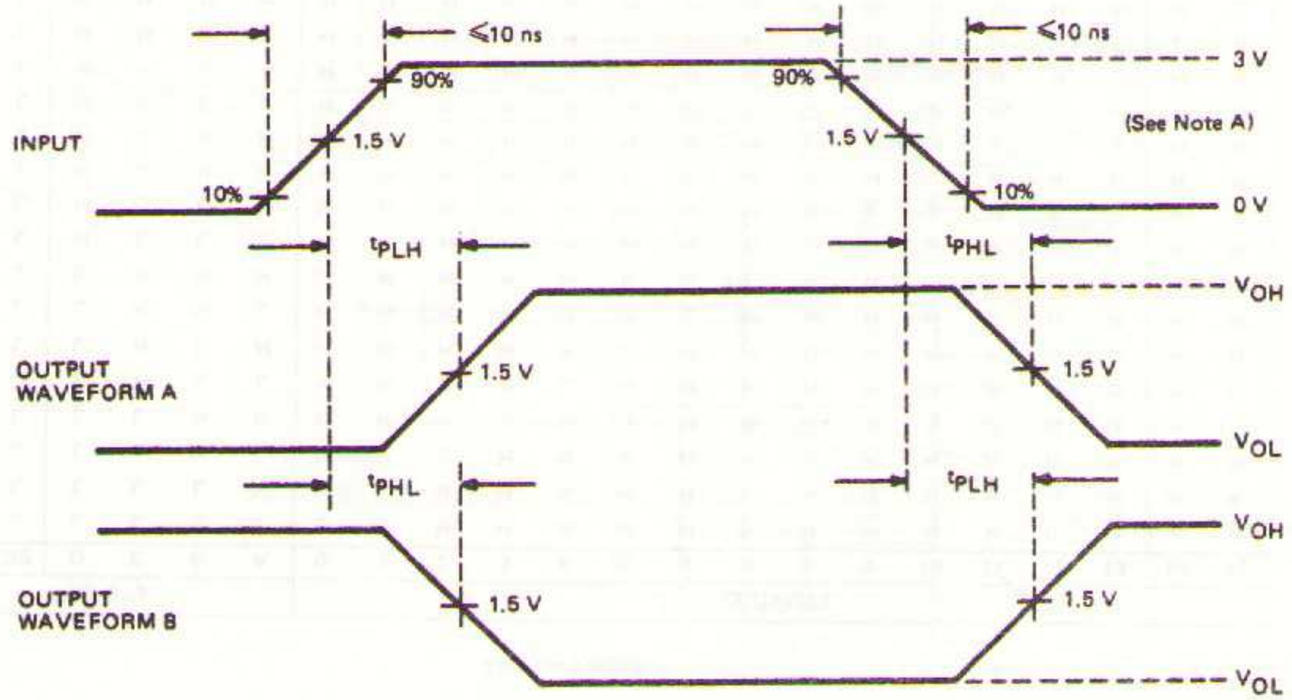
X = irrelevant

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

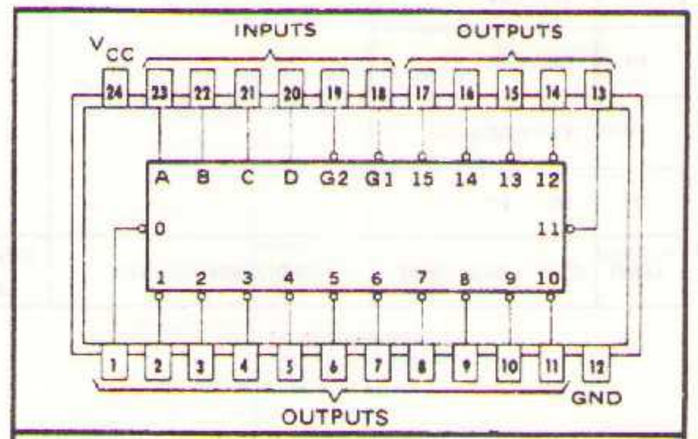
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, duty cycle = 50%, and $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 6—SWITCHING TIMES

FOR APPLICATIONS IN COMMUNICATIONS EQUIPMENT, COMPUTERS, AND ELECTRONIC INSTRUMENTATION

- Decodes 4 binary-coded inputs into one of 16 mutually exclusive outputs
- Performs the demultiplexing function by distributing data from one input line to any one of 16 outputs
- Input clamping diodes simplify system design
- High fan-out, low-impedance, totem-pole outputs
- Typical average propagation delay times:
  23 ns through 3 levels of logic
  19 ns from strobe input
- Typical power dissipation . . . 170 mW
- Fully compatible with most TTL, DTL, and MSI circuits

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table

†Pin assignments for these circuits are the same for all packages.

description

Each of these monolithic, 4-line-to-16-line decoders utilizes TTL circuitry to decode four binary-coded inputs into one of sixteen mutually exclusive outputs when both the strobe inputs, G1 and G2, are low. The demultiplexing function is performed by using the 4 input lines to address the output line, passing data from one of the strobe inputs with the other strobe input low. When either strobe input is high, all outputs are high.

These circuits are fully compatible for use with most other TTL and DTL circuits. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. Input buffers are used to lower the fan-in requirement to only one normalized Series 54/74 load. A fan-out to 10 normalized Series 54/74 loads in the low-level state and 20 in the high-level state is available from each of the sixteen outputs. Typical power dissipation is 170 mW.

The SN54154 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74154 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

INPUTS						OUTPUTS															
G1	G2	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = high, L = low, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54154 Circuits . . . . . −55°C to 125°C
SN74154 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54154			SN74154			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

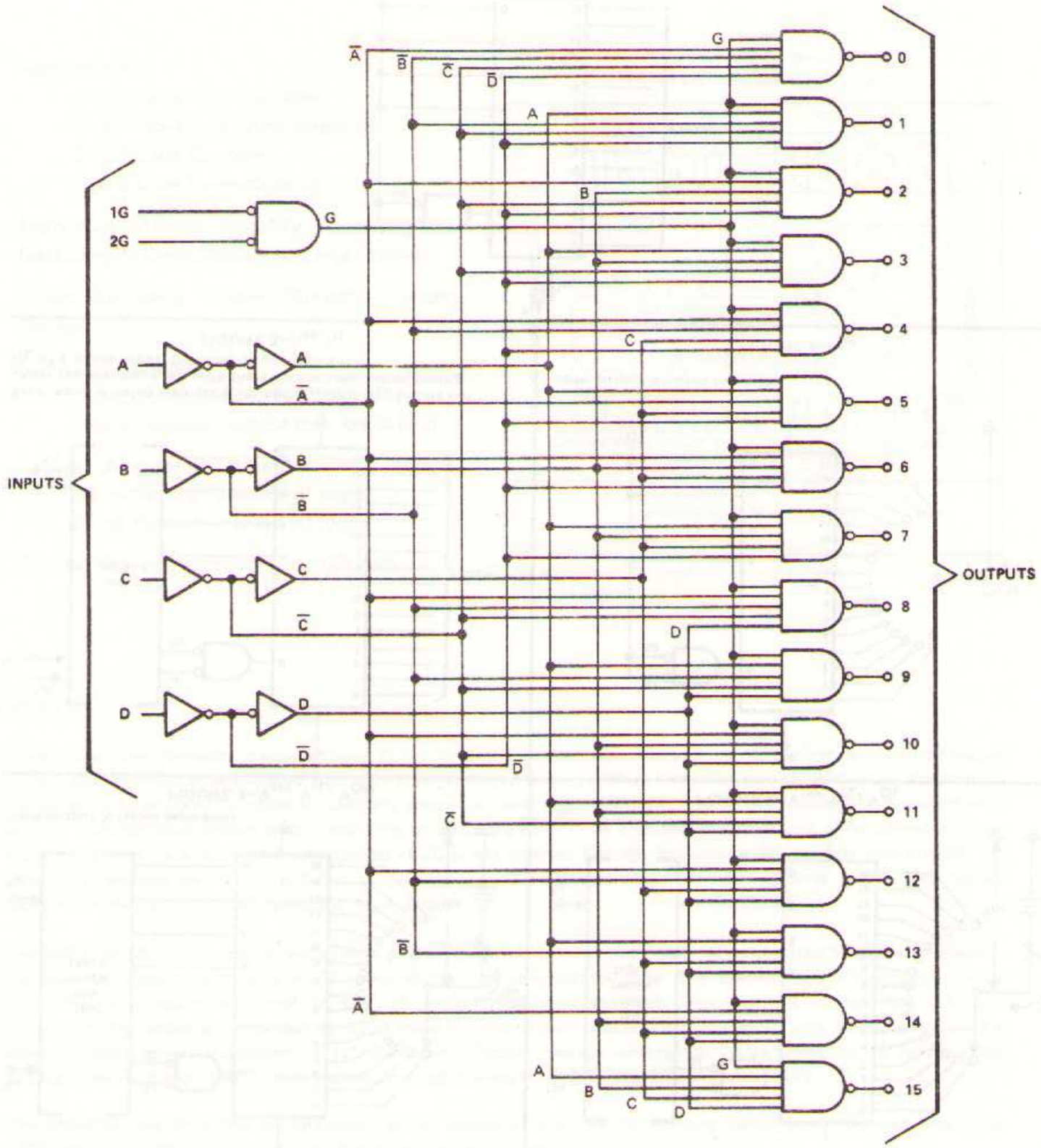
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54154	−20		−55	mA
				SN74154	−18		−57	
I_{CC}	Supply current	5	V_{CC} = MAX	SN54154		34	49	mA
				SN74154		34	56	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

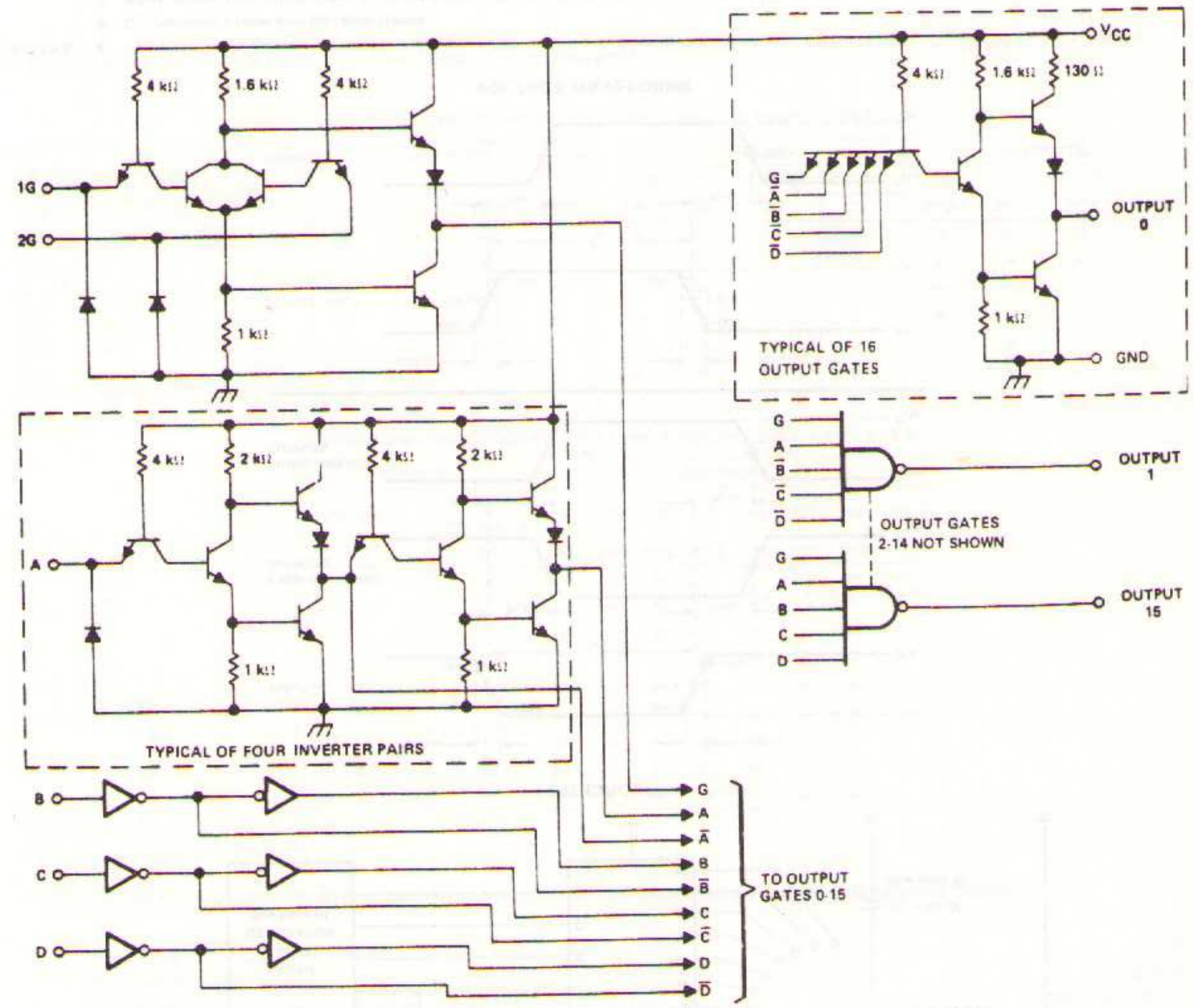
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from A, B, C, or D inputs through 3 levels of logic	6	C_L = 15 pF, R_L = 400 Ω		24	36	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from A, B, C, or D inputs through 3 levels of logic				22	33	ns
t_{PLH}	Propagation delay time, low-to-high-level output, from either strobe input				20	30	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from either strobe input				18	27	ns

functional block diagram



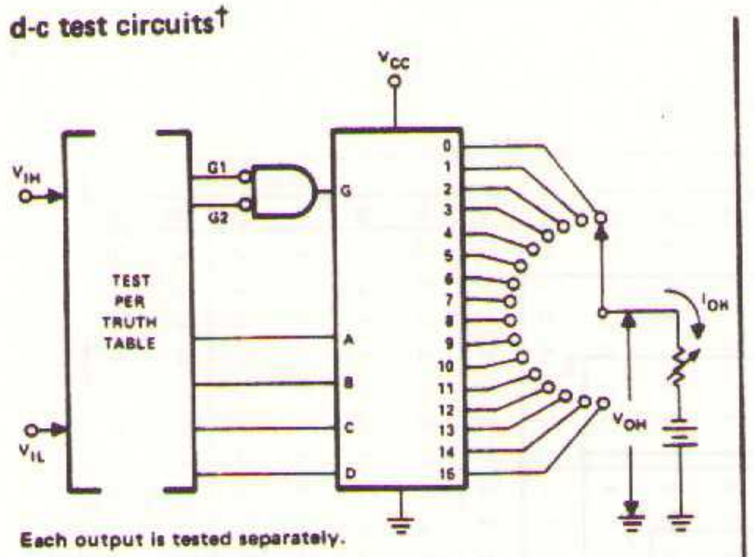
schematic



Component values shown are nominal.

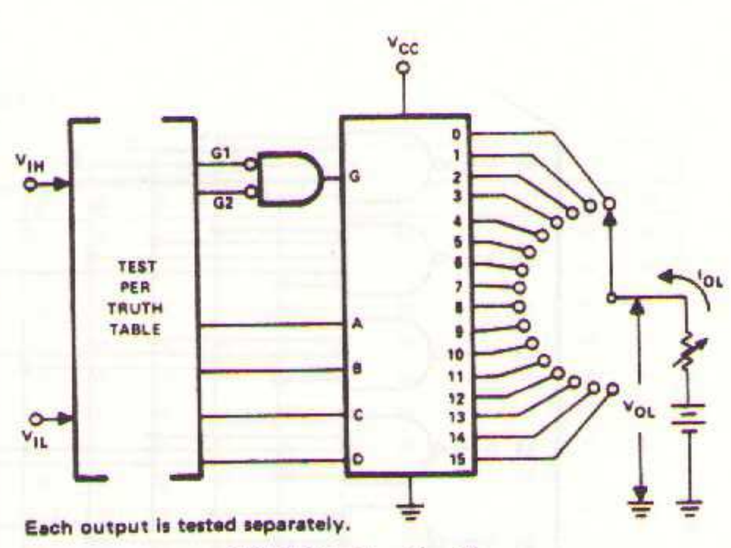
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



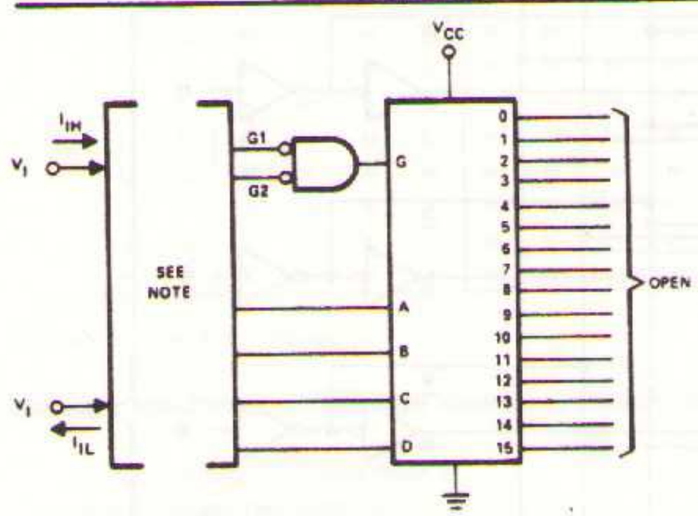
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



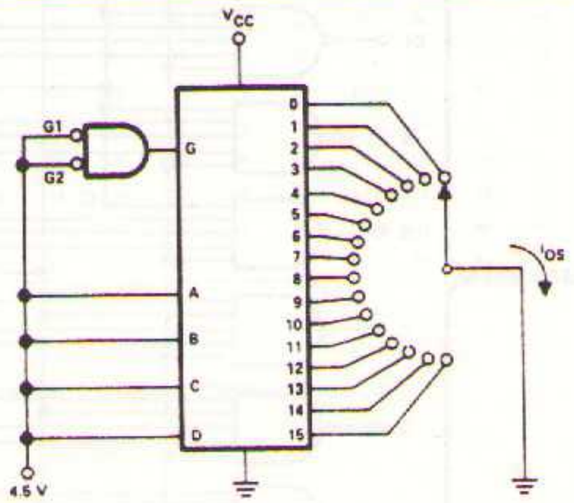
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded, with the exception that when testing I_{IL} of a strobe input, the other strobe is at 2.4 V.

FIGURE 3–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 4–I_{OS}

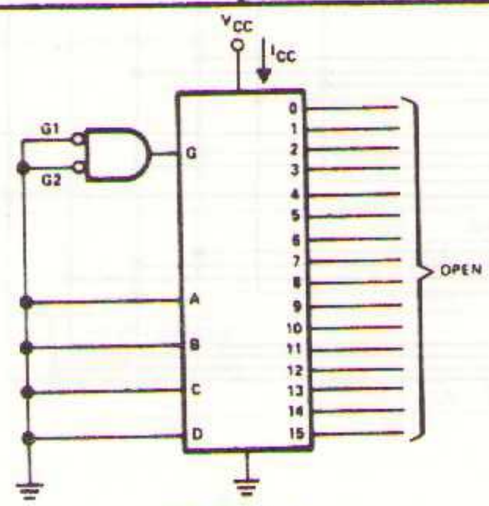
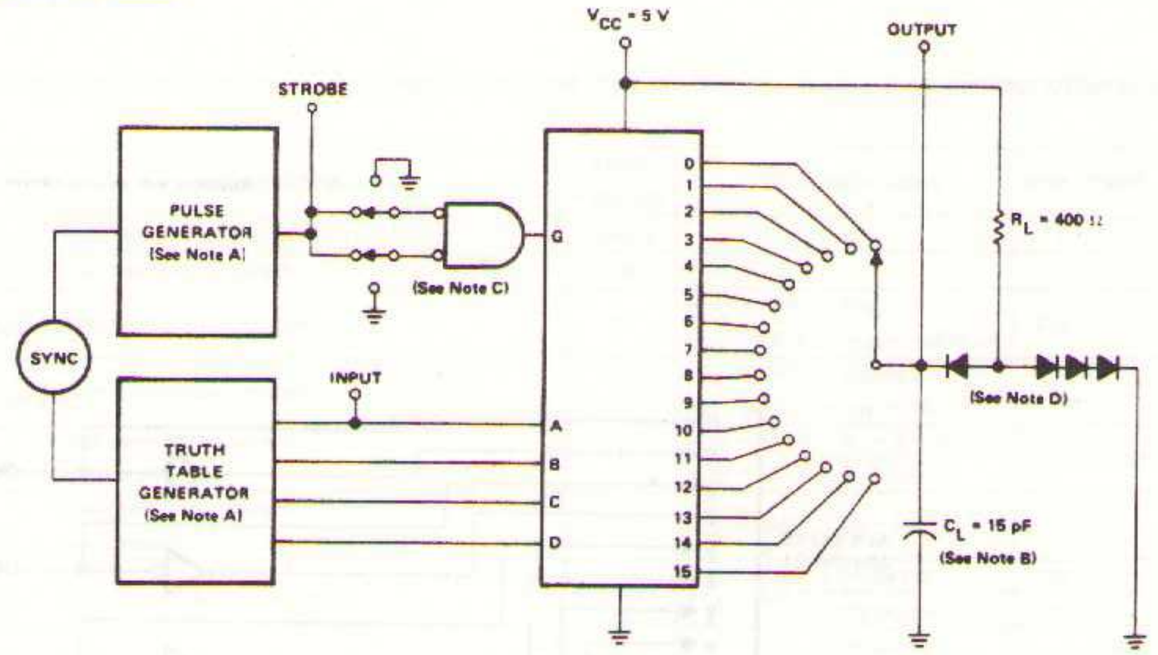


FIGURE 5–I_{CC}

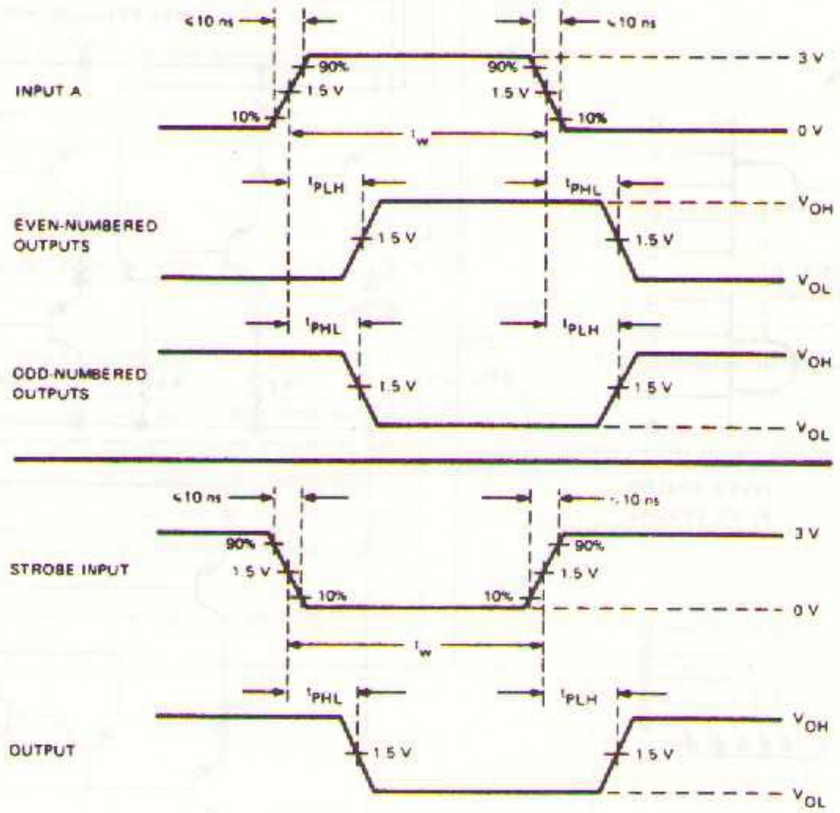
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



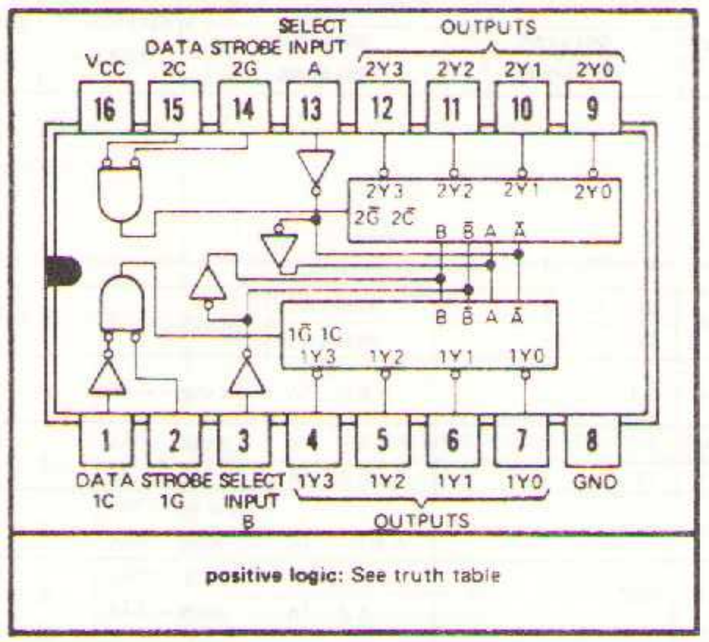
VOLTAGE WAVEFORMS

NOTES: A. The truth table generator and the pulse generator have the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. When measuring select-input-to-output times the strobe inputs are grounded. When measuring strobe-input-to-output times, the untested strobe input is grounded. Select inputs determine output under test through truth table generator.
D. All diodes are 1N3064.

FIGURE 6–SWITCHING TIMES

- Applications:
  - Dual 2-to-4-Line Decoder
  - Dual 1-to-4-Line Demultiplexer
  - 3-to-8-Line Decoder
  - 1-to-8-Line Demultiplexer
- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Input Clamping Diodes Simplify System Design
- Choice of Outputs:
  - Totem Pole (SN54155, SN74155)
  - Open-Collector (SN54156, SN74156)
- Typical Average Propagation Delay Times:
  - 16 ns through 2 levels of logic
  - 21 ns through 3 levels of logic
- Typical Power Dissipation . . . 125 mW

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These monolithic transistor-transistor-logic (TTL) circuits feature dual 1-line-to-4-line demultiplexers with individual strobes and common binary-address inputs in a single 16-pin package. When both sections are enabled by the strobes, the common binary-address inputs sequentially select and route associated input data to the appropriate output of each section. The individual strobes permit activating or inhibiting each of the 4-bit sections as desired. Data applied to input 1C is inverted at its outputs and data applied at 2C is not inverted through its outputs. The inverter following the 1C data input permits use as a 3-to-8-line decoder or 1-to-8-line demultiplexer without external gating. See typical applications data and the truth tables for more details.

The SN54155/SN74155 circuits, with totem-pole outputs, are rated to fan-out to 10 normalized Series 54/74 loads in the low-level output state, and to 20 loads in the high-level output state. The SN54156/SN74156 circuits, with open-collector outputs, are rated to sink 16 milliamperes at a low-level output voltage of less than 0.4 volt. Input-clamping diodes are provided on all of these circuits to minimize transmission-line effects and simplify system design. Typical power dissipation is 125 milliwatts. Typical average propagation delay times are 16 nanoseconds through 2 levels of logic and 21 nanoseconds through 3 levels of logic for the SN54155/SN74155.

The SN54155 and SN54156 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74155 and SN74156 are characterized for operation from 0°C to 70°C.

truth tables (H = high level, L = low level, X = irrelevant)

2-LINE-TO-4-LINE DECODER OR 1-LINE-TO-4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	1G	1C	1Y0	1Y1	1Y2	1Y3
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

INPUTS				OUTPUTS			
SELECT		STROBE	DATA				
B	A	2G	2C	2Y0	2Y1	2Y2	2Y3
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE-TO-8-LINE DECODER TO 1-LINE-TO-8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE OR DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

†C = inputs 1C and 2C connected together
‡G = inputs 1G and 2G connected together

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Operating free-air temperature range:	SN54155, SN54156 Circuits	−55°C to 125°C
	SN74155, SN74156 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54155			SN74155			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		55	25	125	0	25	70	°C

	SN54156			SN74156			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature range, T_A	−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54155, SN74155 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	SN54155	−20		−55	mA
				SN74155	−18		−57	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54155		25	35	mA
				SN74155		25	40	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		SN54156, SN74156 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	2 and 3			2			V
V_{IL}	Low-level input voltage	2					0.8	V
I_{OH}	High-level output current	3	V_{CC} = MIN, V_I = 2 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (each input)	4	V_{CC} = MAX, V_I = 2.4 V				40	μA
			V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (each input)	4	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{CC}	Supply current	6	V_{CC} = MAX	SN54156		25	35	mA
				SN74156		25	40	

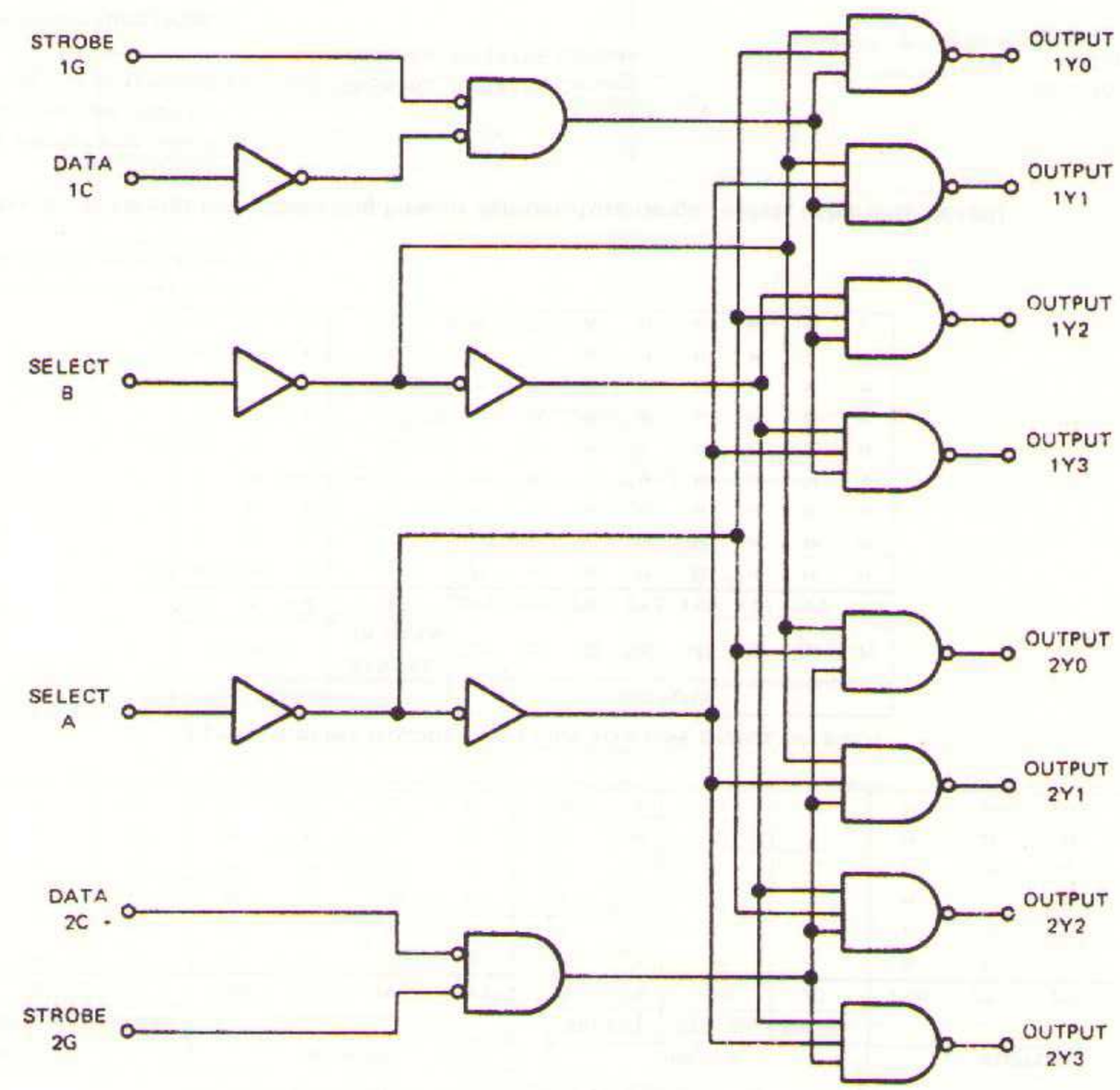
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

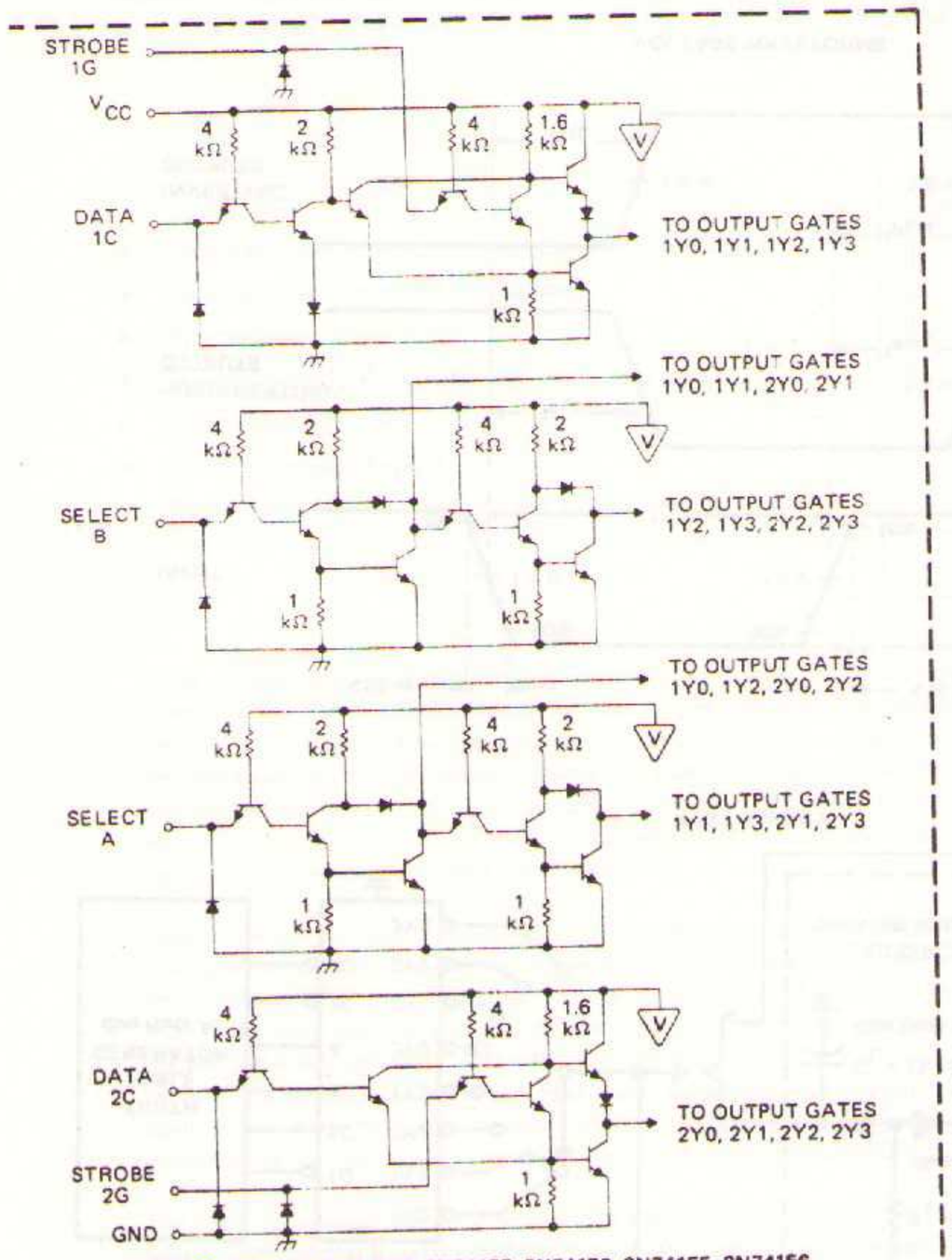
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	LEVELS OF LOGIC	TEST FIGURE	TEST CONDITIONS	SN54155 SN74155 MIN	TYP	MAX	SN54156 SN74156 MIN	TYP	MAX	UNIT
t_{PLH}	A, B, 2C, 1G, or 2G	Y	2	7	C_L = 15 pF, R_L = 400 Ω		13	20		15	23	ns
t_{PHL}	A, B, 2C, 1G, or 2G	Y	2				18	27		20	30	ns
t_{PLH}	A or B	Y	3				21	32		23	34	ns
t_{PHL}	A or B	Y	3				21	32		23	34	ns
t_{PLH}	1C	Y	3				16	24		18	27	ns
t_{PHL}	1C	Y	3				20	30		22	33	ns

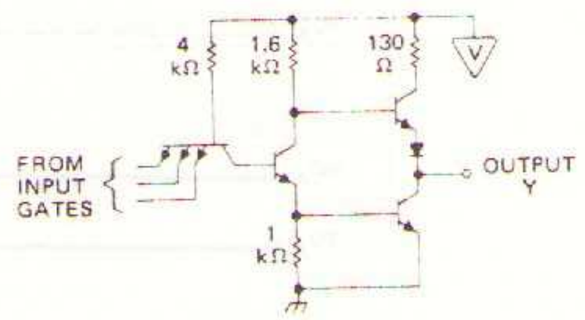
¶t_{PLH} propagation delay time, low-to-high-level output
t_{PHL} propagation delay time, high-to-low-level output

functional block diagram

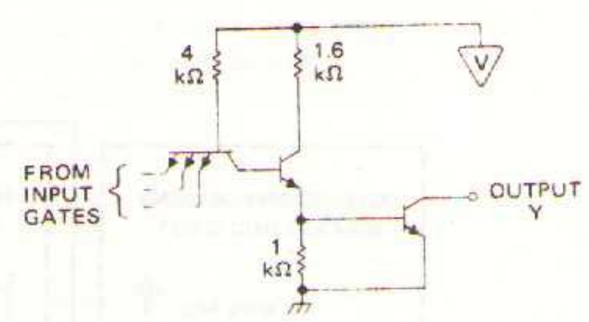




ADDRESS INPUT GATES FOR SN54155, SN54156, SN74155, SN74156



OUTPUT GATE FOR SN54155, SN74155 (ONE OF EIGHT SHOWN)



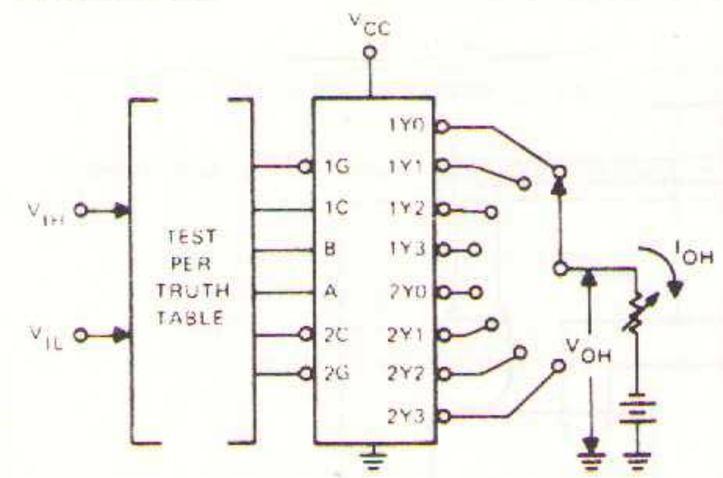
OUTPUT GATE FOR SN54156, SN74156 (ONE OF EIGHT SHOWN)

Component values shown are nominal.

V ... V_{CC} bus

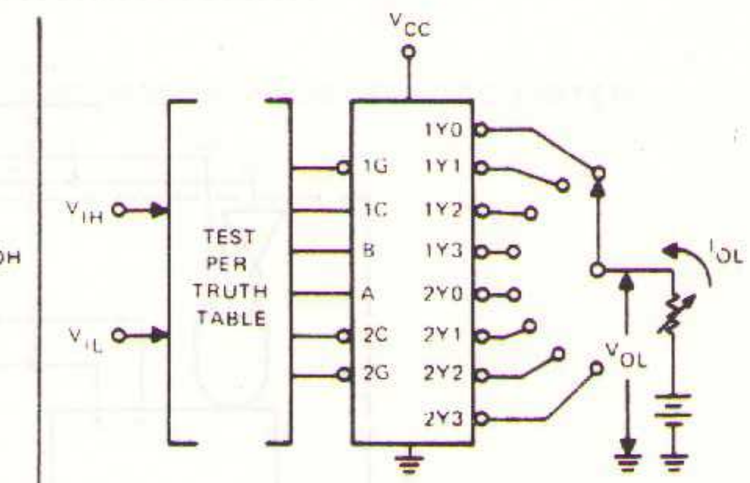
PARAMETER MEASUREMENT INFORMATION

d-c test circuits†



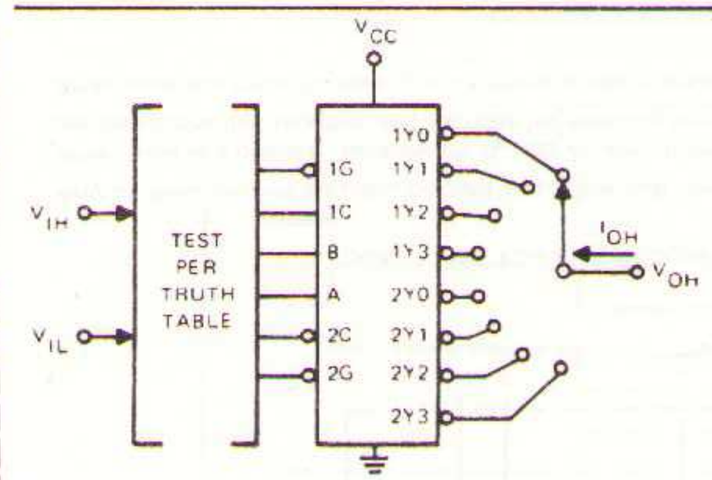
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



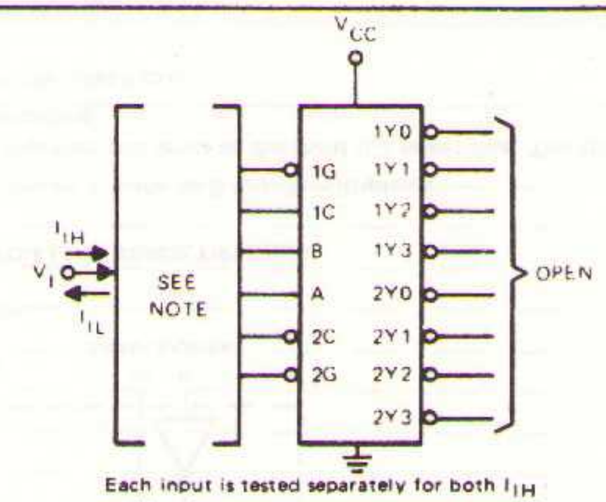
Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



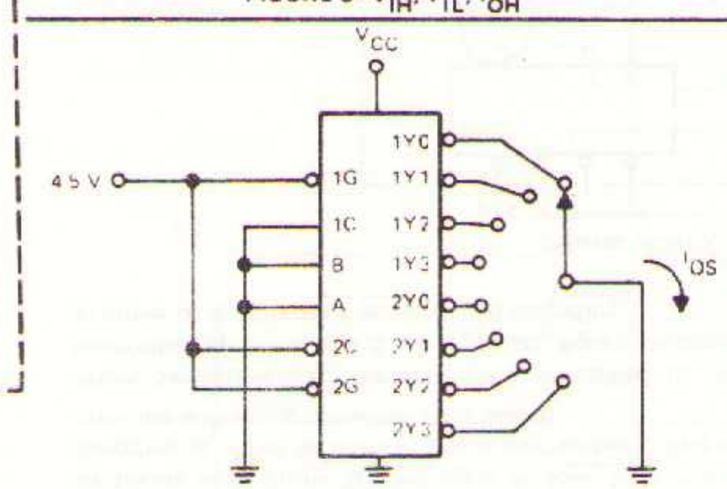
Each output is testec separately.

FIGURE 3–V_{IH}, V_{IL}, I_{OH}



Each input is tested separately for both I_{IH} and I_{IL}. Inputs not under test are grounded.

FIGURE 4–I_{IH}, I_{IL}



Each output is tested separately.

FIGURE 5–I_{OS}

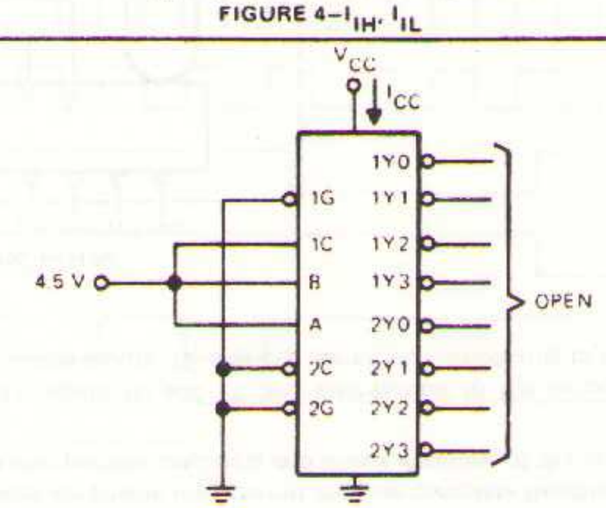
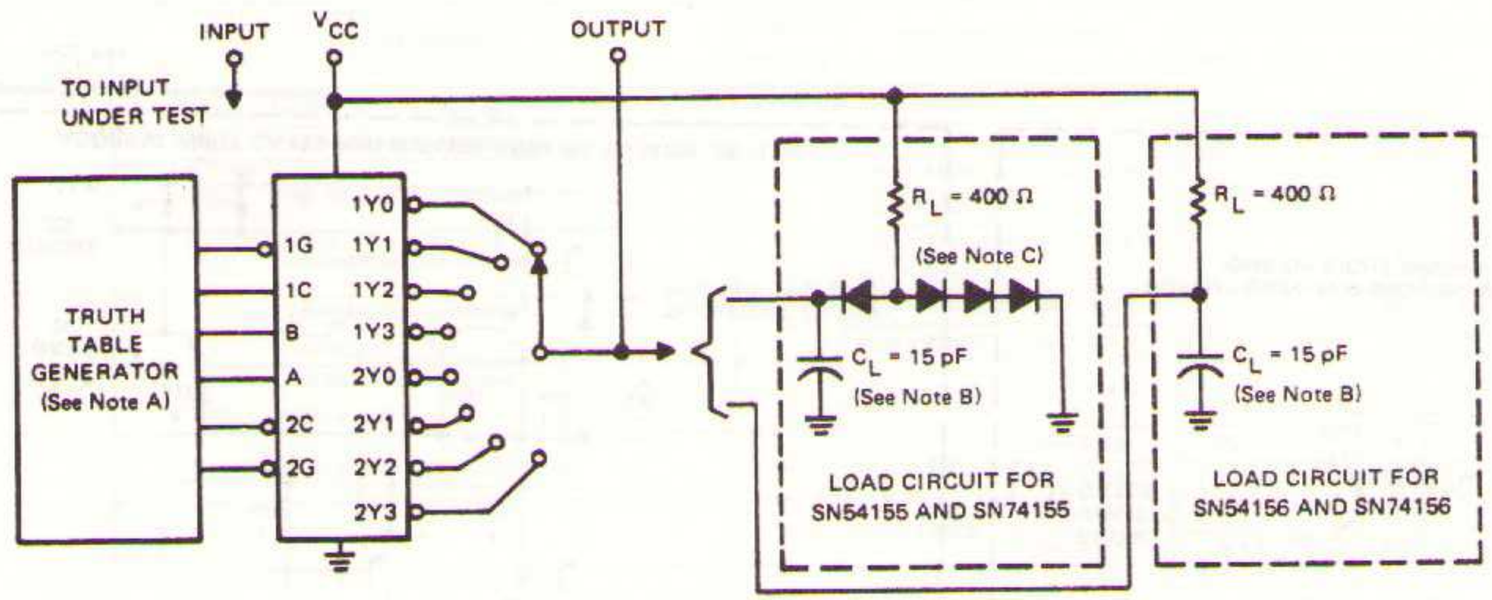


FIGURE 6–I_{CC}

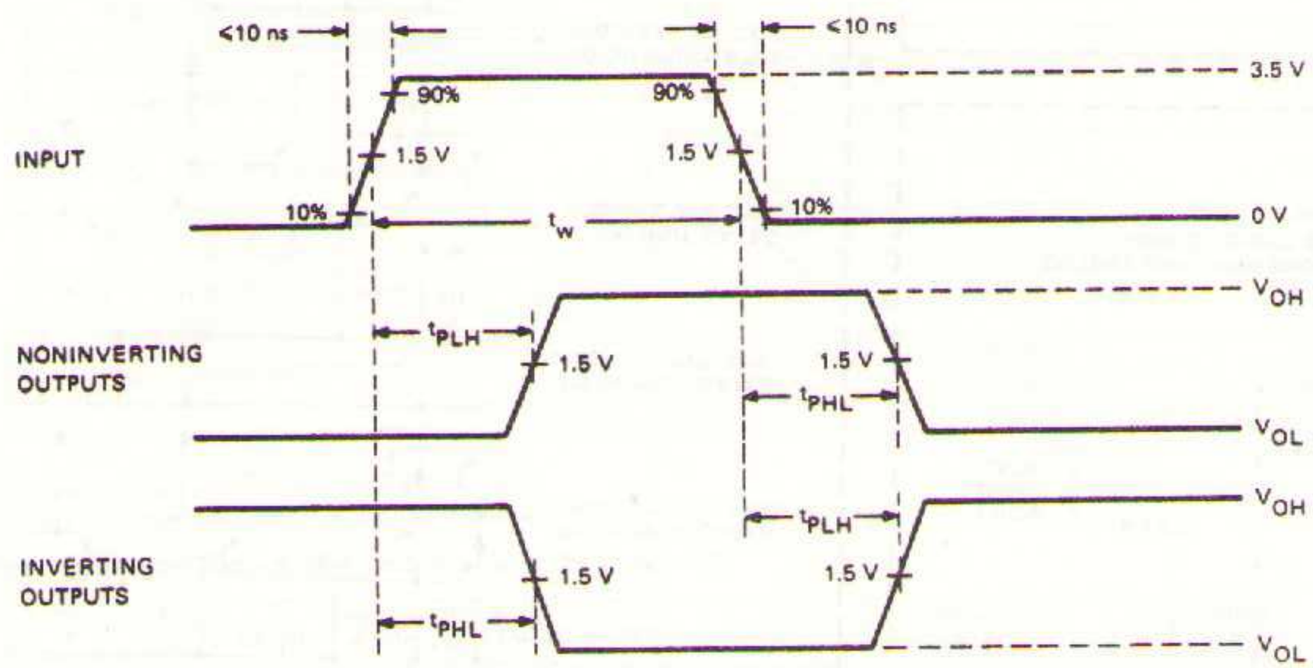
† Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The truth table generator has the following characteristics: PRR = 1 MHz; $Z_{out} \approx 50\ \Omega$, t_w = 100 ns.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

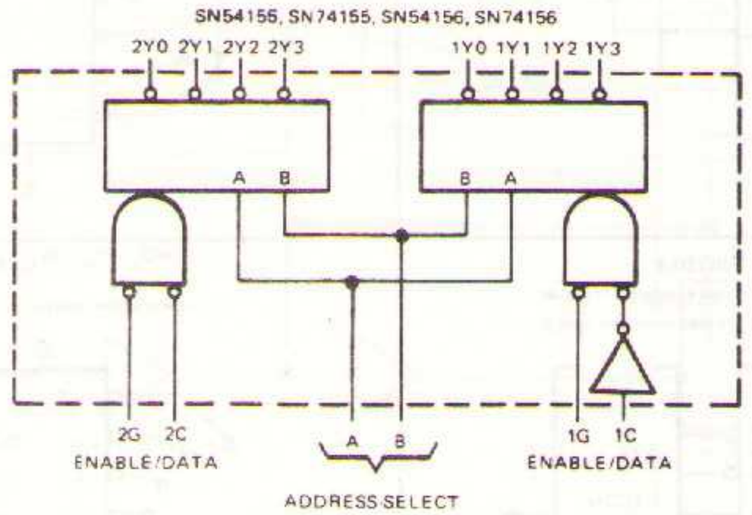
FIGURE 7—PROPAGATION DELAY TIME

TYPICAL APPLICATION DATA

THE SN54155, SN74155, SN54156, or SN74156 may be used as a dual 2-line-to-4-line decoder or a 1-line-to-4-line demultiplexer. These applications are identical except as follows:

When decoding, the 2-line code is applied to select inputs A and B. The 4-line output section (1Y0, 1Y1, 1Y2, 1Y3) is enabled by taking strobe 1G low and input 1C high. The other 4-line output section (2Y0, 2Y1, 2Y2, 2Y3) is enabled by taking both strobe 2G and input 2C low. Note that the separate enable lines permit the user complete flexibility in decoding at either or both of the output sections. The strobe also permits cascading and allows disabling of the circuits until the addressing transients have passed.

When demultiplexing, the serial data is applied to the data inputs 1C and 2C and distribution to the outputs is controlled by the A and B select inputs. Again, the separate strobe inputs, 1G and 2G, permit demultiplexing to occur at either or both output sections, and cascading.

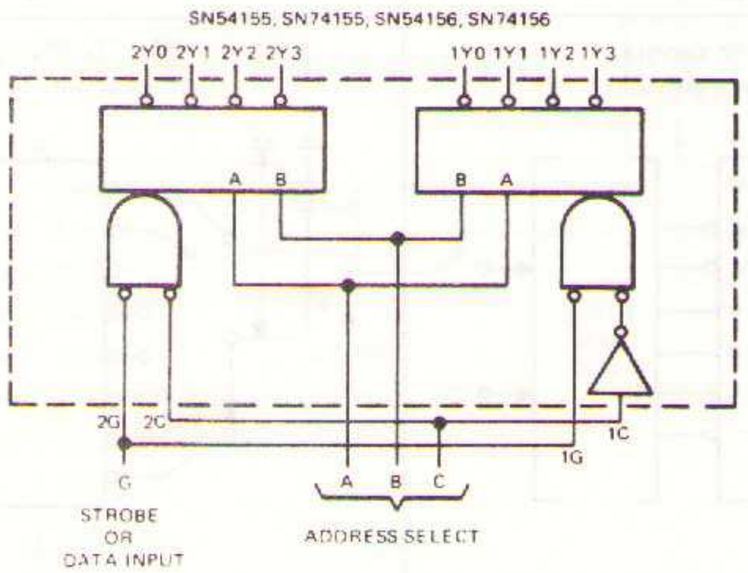


DUAL 2-LINE-TO-4-LINE DECODER/1-TO-4-LINE DEMULTIPLEXER

Any of these circuits may also be used as a 3-line-to-8-line decoder or a 1-line-to-8-line demultiplexer.

When used as a decoder, data inputs 1C and 2C are connected together and serve as the third (C) select line. The strobes are also connected together and are used for enabling and/or cascading.

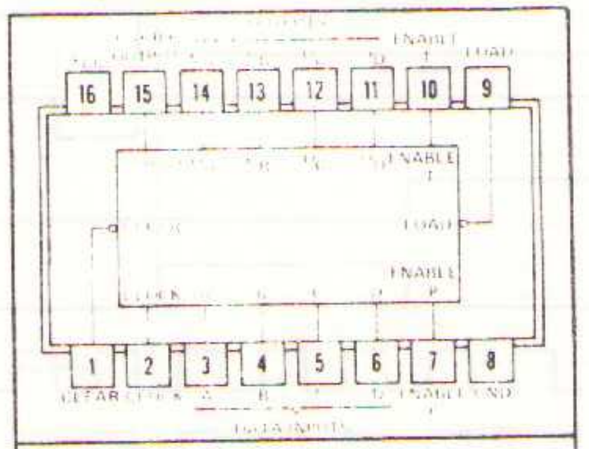
When used as a demultiplexer, the common strobe line serves as the data input.



3-LINE-TO-8-LINE DECODER/1-TO-8-LINE DEMULTIPLEXER

SN54160, SN54161, SN74160, SN74161, . . . SYNCHRONOUS COUNTERS WITH DIRECT CLEAR
SN54162, SN54163, SN74162, SN74163 . . . FULLY SYNCHRONOUS COUNTERS

J OR N DUAL IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

† Pin assignments for these circuits are the same for all packages.

- Internal Look-Ahead for Fast Counting Schemes
- Carry Output for n-Bit Cascading
- Synchronous Counting
- Synchronously Programmable
- Load Control Line
- Diode-Clamped Inputs
- Typical Maximum Input Clock Frequency . . . 32 MHz

description

These synchronous, presettable counters feature an internal carry look-ahead for application in high-speed counting schemes. The SN54160, SN54162, SN74160, and SN74162 are decade counters and the SN54161, SN54163, SN74161, and SN74163 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the four J-K master-slave flip-flops on the rising (positive-going) edge of the clock input waveform.

These counters are fully programmable; that is, the outputs may be preset to either state. As presetting is synchronous, placing a low level on the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse. The clear function for the SN54160, SN54161, SN74160, and SN74161 is asynchronous and a low level at the clear input sets all four of the flip-flop outputs low regardless of the state of the clock. The clear function for the SN54162, SN54163, SN74162, and SN74163 is synchronous and a low level at the clear input sets all four of the flip-flop outputs low after the next clock pulse. This synchronous clear allows the count length to be modified easily as decoding the maximum count desired can be accomplished with one external NAND gate. The gate output is connected to the clear input to synchronously set the counter to 0000 (LLLL).

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count-enable inputs (P and T) must be high to count, and input T is fed forward to enable the carry output. The carry output thus enabled will produce a positive output pulse with a duration approximately equal to the positive portion of the Q_A output. This positive overflow carry pulse can be used to enable successive cascaded stages. High-to-low-level transitions at the enable P or T inputs should occur only when the clock input is high.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. A full fan-out to ten normalized Series 54/74 loads is available from each of the outputs in the low-level state. A fan-out to 20 normalized Series 54/74 loads is provided in the high-level state to facilitate connection of unused inputs to used inputs. Input clock frequency is typically 32 megahertz and power dissipation is typically 325 milliwatts.

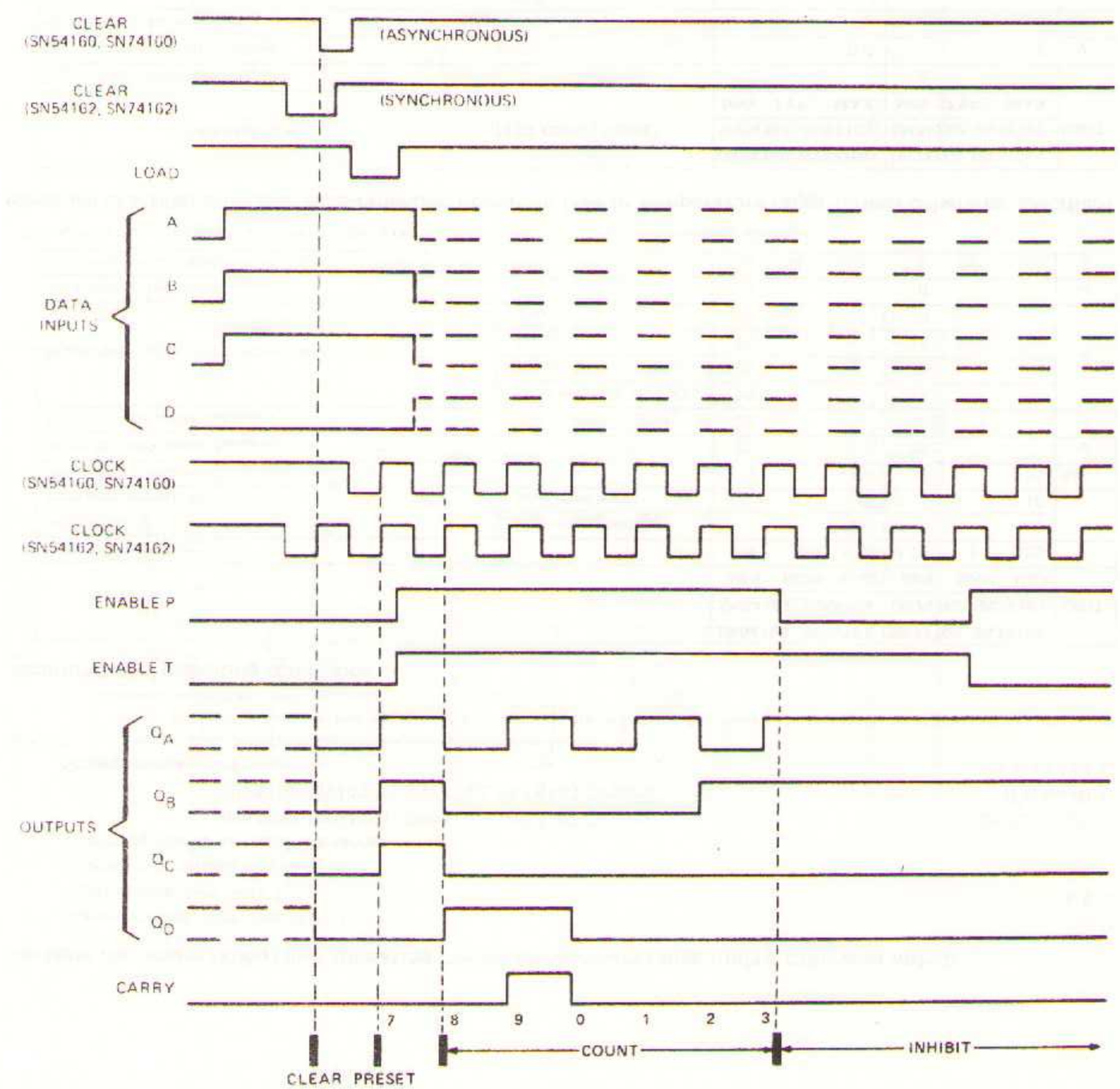
Series 54 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; Series 74 circuits are characterized for operation from 0°C to 70°C.

SN54160, SN54162, SN74160, SN74162 SYNCHRONOUS DECADE COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to BCD seven.
3. Count to eight, nine, zero, one, two, and three.
4. Inhibit

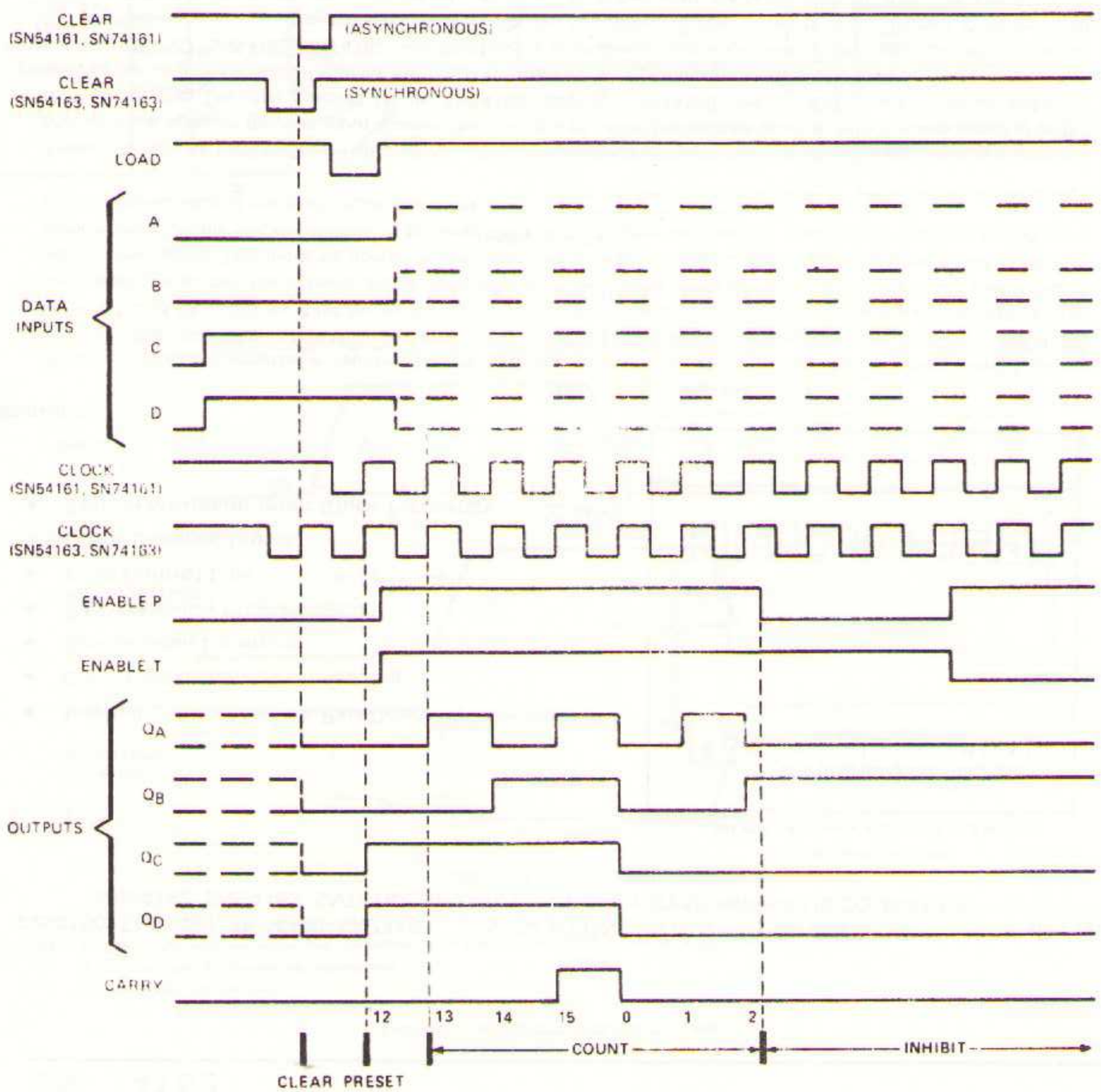


SN54161, SN54163, SN74161, SN74163 SYNCHRONOUS BINARY COUNTERS

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Preset to binary twelve.
3. Count to thirteen, fourteen, fifteen, zero, one, and two.
4. Inhibit.



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range:	
SN54160, SN54161, SN54162, SN54163 Circuits	−55°C to 125°C
SN74160, SN74161, SN74162, SN74163 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the count enable inputs P and T.

recommended operating conditions

		SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$		25			25			ns
Width of clear pulse, $t_{w(clear)}$		20			20			ns
Setup time, t_{setup} (see Figures 1 and 3)	Data inputs A, B, C, D	15			15			ns
	Enable P	20			20			
	Load	15			15			
	Clear	20			20			
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	C

This applies only for SN54162, SN54163, SN74162, and SN74163 which have synchronous clear inputs.

electrical characteristics over recommended operating free-air temperature range (unless otherwise specified)

PARAMETER			TEST CONDITIONS†	SN54160, SN54161, SN54162, SN54163			SN74160, SN74161, SN74162, SN74163			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	Clock or enable T	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
		Other inputs				40			40	
I_{IL}	Low-level input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
		Other inputs				−1.6			−1.6	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 3		59	85		59	94	mA
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 4		63	91		63	101	mA

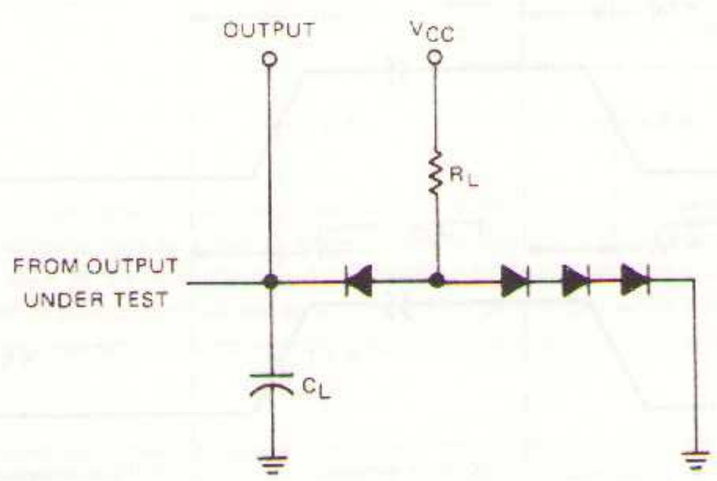
†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

NOTES: 3. I_{CCH} is measured with the load input high, then again with the load input low, with all other inputs high and all outputs open.
4. I_{CCL} is measured with the clock input high, then again with the clock input low, with all other inputs low and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	1,2	C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{PLH}	Propagation delay time, low-to-high-level carry output from clock	1,2			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from clock	1,2			23	35	ns
t_{PLH}	Propagation delay time, low-to-high-level Q output from clock	1,2			13	20	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clock	1,2			15	23	ns
t_{PLH}	Propagation delay time, low-to-high-level carry output from enable T	1,3			8	13	ns
t_{PHL}	Propagation delay time, high-to-low-level carry output from enable T	1,3			10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level Q output from clear	1,3			20	30	ns

PARAMETER MEASUREMENT INFORMATION

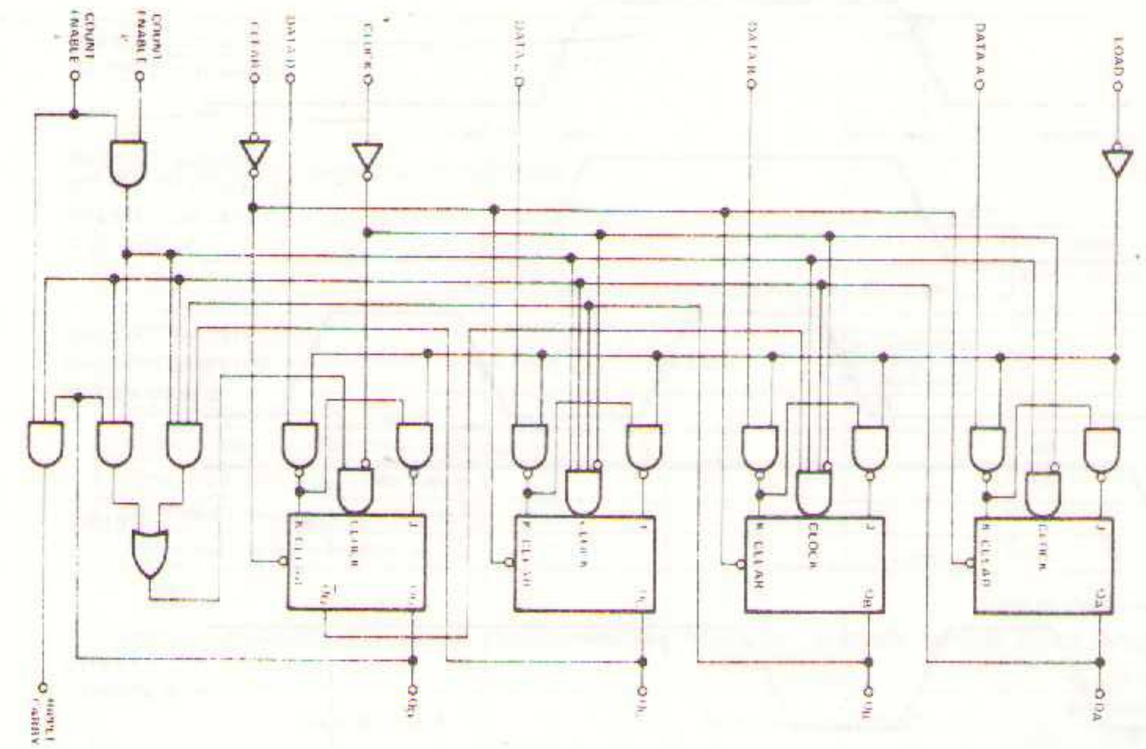


NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.

LOAD CIRCUIT FOR SWITCHING TESTS
FIGURE 1

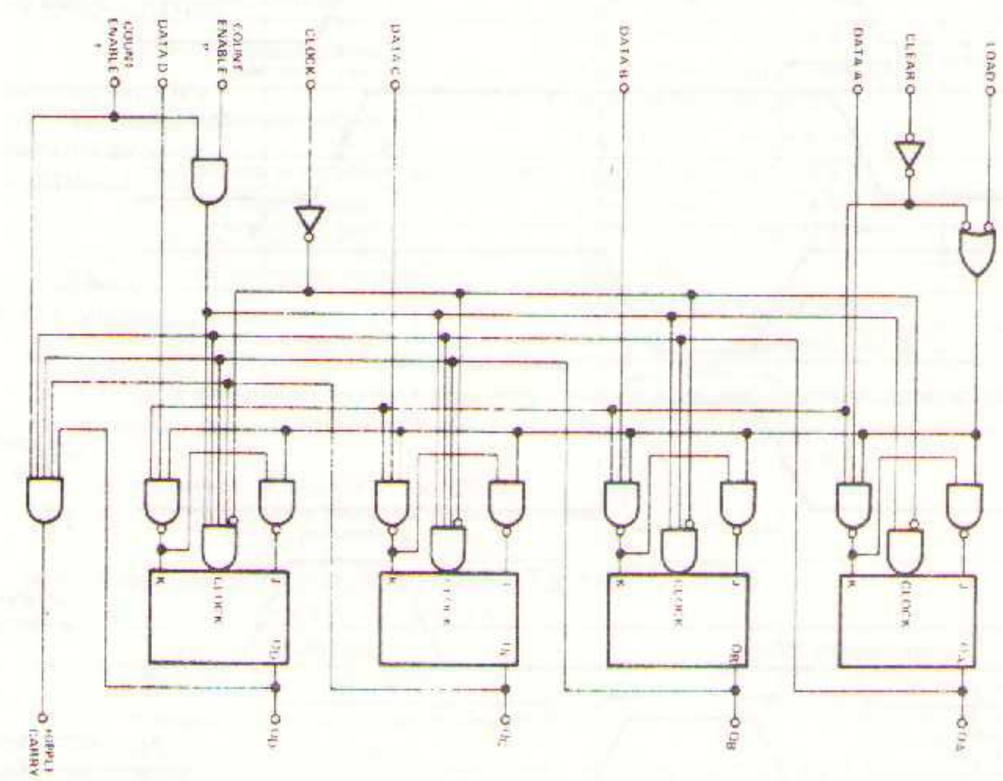
SN54160, SN74160 SYNCHRONOUS DECADE COUNTERS

SN54162, SN74162 synchronous decade counters are similar; however, the clear is synchronous as shown for the SN54163, SN74163 binary counters at right.

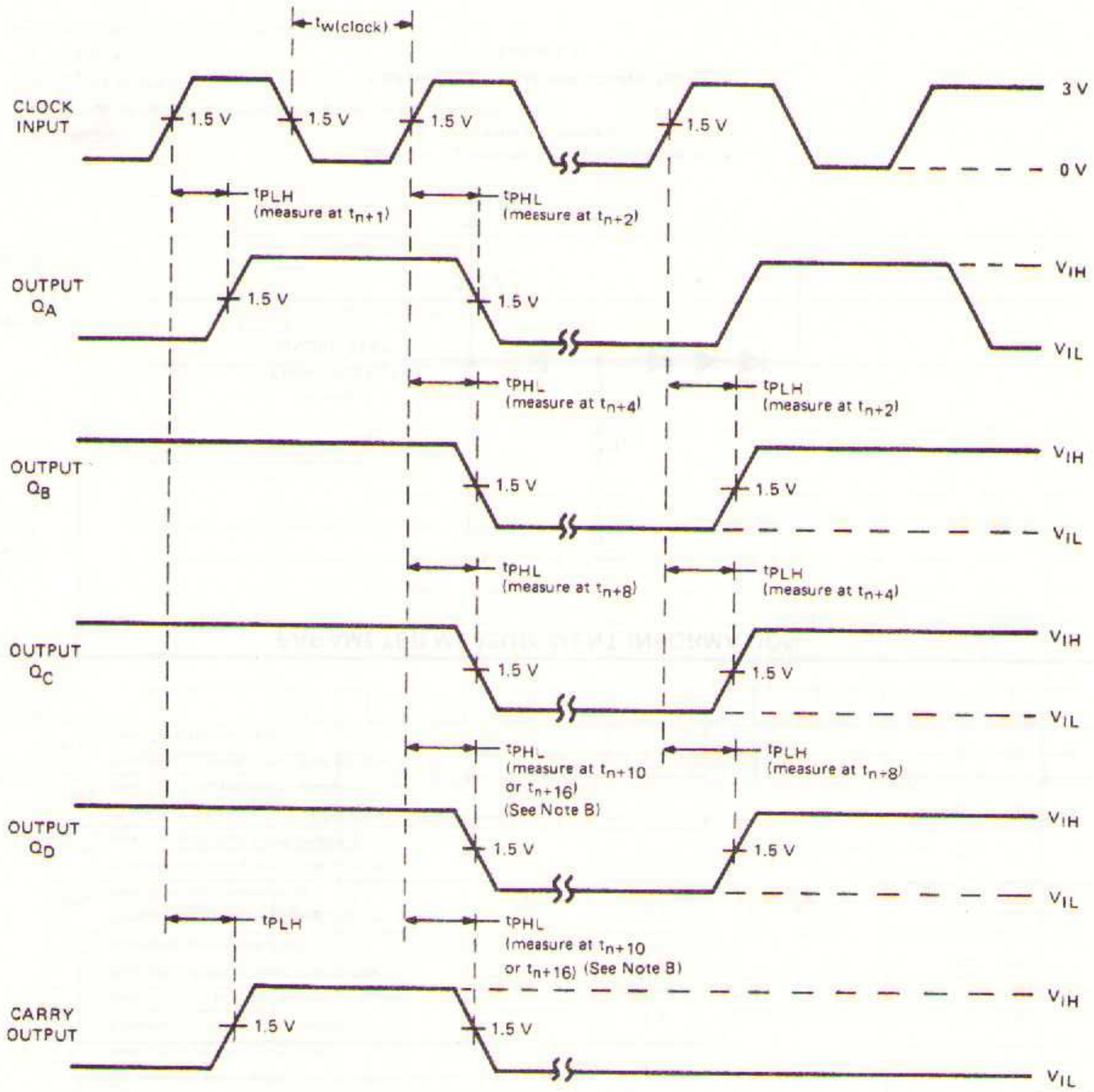


SN54161, SN74161 SN54163, SN74163 SYNCHRONOUS BINARY COUNTERS

SN54161, SN74161 synchronous binary counters are similar; however, the clear is asynchronous as shown for the SN54160, SN74160 decade counters at left.



PARAMETER MEASUREMENT INFORMATION



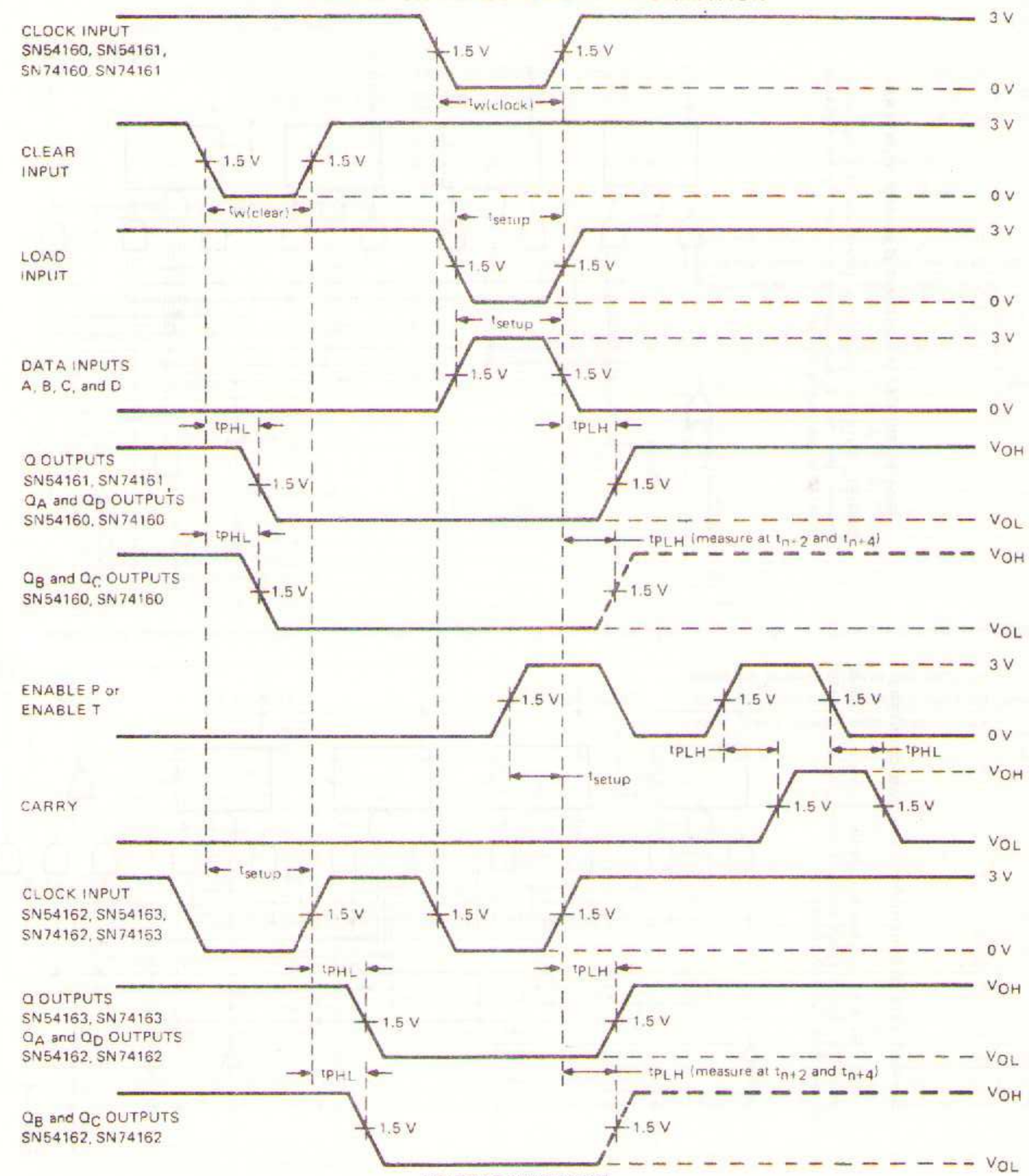
VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$. Vary PRR to measure f_{max}.

B. Outputs Q_D and carry are tested at t_{n+10} for the SN54163, SN54162, SN74160, and SN74162, and at t_{n+16} for the SN54161, SN54163, SN74161, and SN74163, where t_n is the bit time when all outputs are low.

FIGURE 2–SWITCHING TIMES

PARAMETER MEASUREMENT INFORMATION



VOLTAGE WAVEFORMS

NOTES: A. The input pulses are supplied by a generator having the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR ≤ 1 MHz, duty cycle $\leq 50\%$, $Z_{out} \approx 50\ \Omega$.

B. Enable P and enable T setup times are measured at $t_n = 0$.

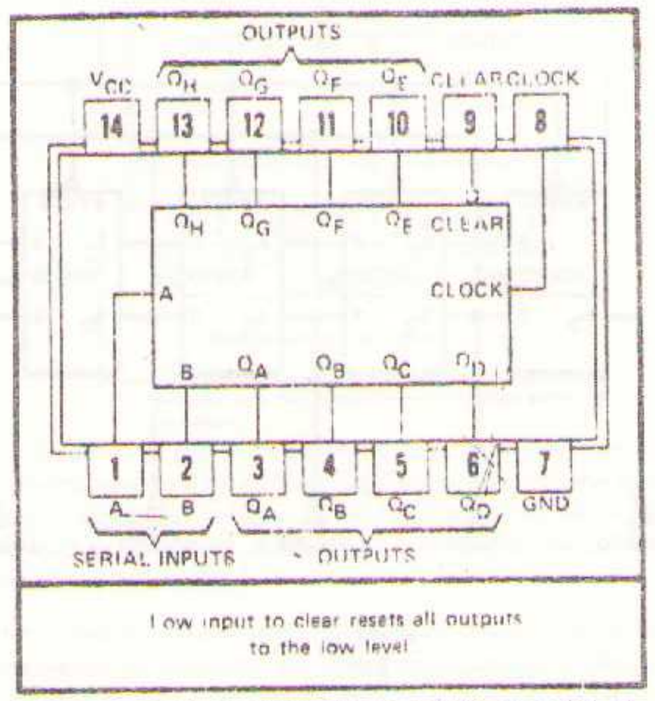
FIGURE 3–SWITCHING TIMES

- Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Asynchronous Clear
- Typical Maximum Input Clock Frequency . . . 36 MHz

TRUTH TABLE
SERIAL INPUTS A AND B

INPUTS AT t_n		OUTPUT AT t_{n+1}
A	B	Q_A
H	H	H
L	H	L
H	L	L
L	L	L

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



Low input to clear resets all outputs to the low level

†Pin assignments for these circuits are the same for all packages.

description

These 8-bit shift registers feature gated serial inputs and an asynchronous clear. The gated serial inputs (A and B) permit complete control over incoming data as a low at either (or both) input(s) inhibits entry of the new data and resets the first flip-flop to the low level at the next clock pulse. A high-level input enables the other input which will then determine the state of the first flip-flop. Data at the serial inputs may be changed while the clock is high, but only information meeting the setup requirements will be entered. Clocking occurs on the low-to-high-level transition of the clock input.

All inputs are diode-clamped to minimize transmission-line effects, and are buffered to represent only one Series 54/74 load which simplifies system design. Power dissipation is typically 21 milliwatts per bit. Maximum input clock frequency is typically 36 megahertz.

The SN54164 is characterized for operation over the full military temperature range of -55°C to 125°C; the SN74164 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54164 Circuits . . . . . −55°C to 125°C
SN74164 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54164 MIN	SN54164 NOM	SN54164 MAX	SN74164 MIN	SN74164 NOM	SN74164 MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			10			10	
	Low logic level			5			5	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear input pulse, t_w		20			20			ns
Data setup time, t_{setup} (see Figure 1)		15			15			ns
Data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54164 MIN	SN54164 TYP‡	SN54164 MAX	SN74164 MIN	SN74164 TYP‡	SN74164 MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX,	I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 8 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−10		−27.5	−9		−27.5	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2	$V_{I(clock)}$ = 0.4 V		30			30		mA
			$V_{I(clock)}$ = 2.4 V		37	54		37	54	

NOTE 2: I_{CC} is measured with outputs open, serial inputs grounded, and a momentary ground, then 4.5 V, applied to clear.

†For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

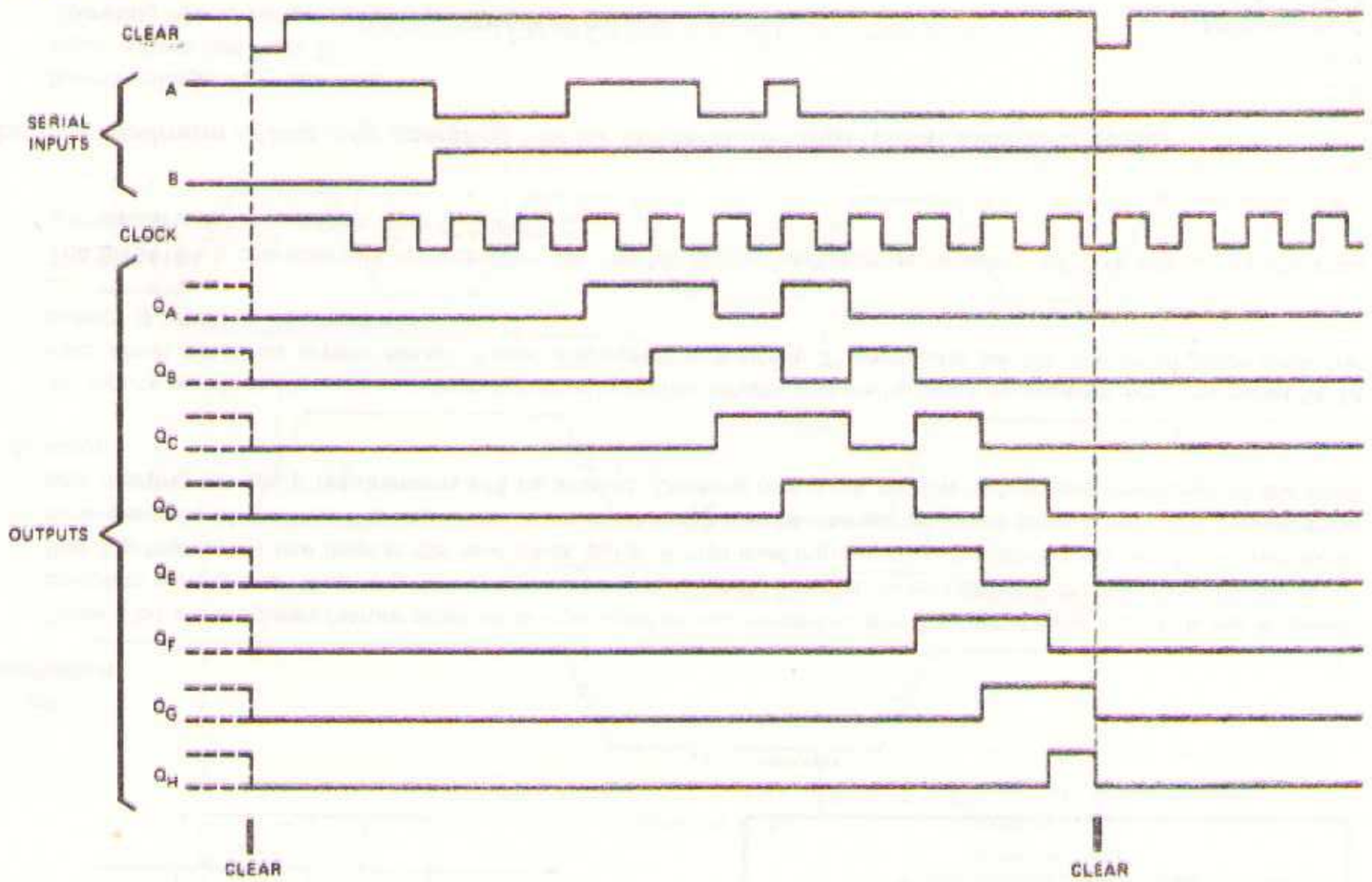
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than two outputs should be shorted at a time.

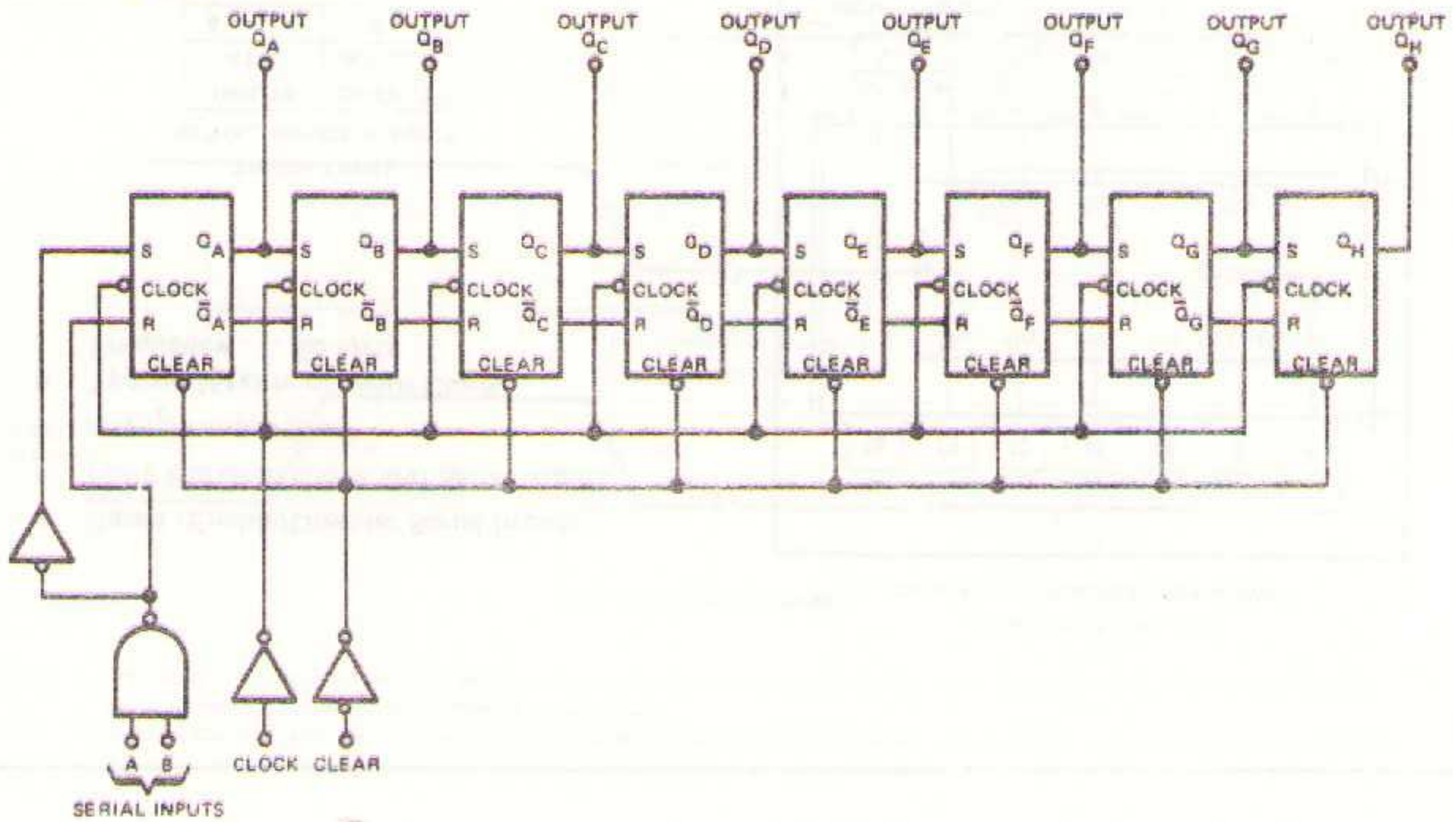
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 5

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	R_L = 800 Ω, See Figure 1	C_L = 15 pF	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clear input		C_L = 15 pF		24	36	ns
			C_L = 50 pF		28	42	
t_{PLH}	Propagation delay time, low-to-high-level Q outputs from clock input		C_L = 15 pF	8	17	27	ns
			C_L = 50 pF	10	20	30	
t_{PHL}	Propagation delay time, high-to-low-level Q outputs from clock input		C_L = 15 pF	10	21	32	ns
			C_L = 50 pF	10	25	37	

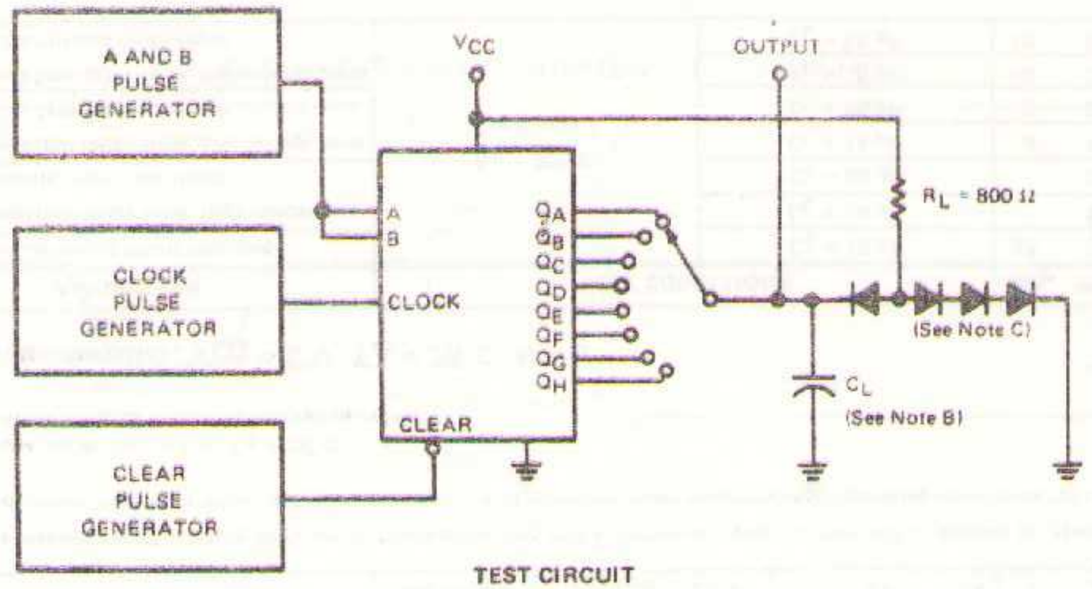
typical clear, inhibit, shift, clear, and inhibit sequences



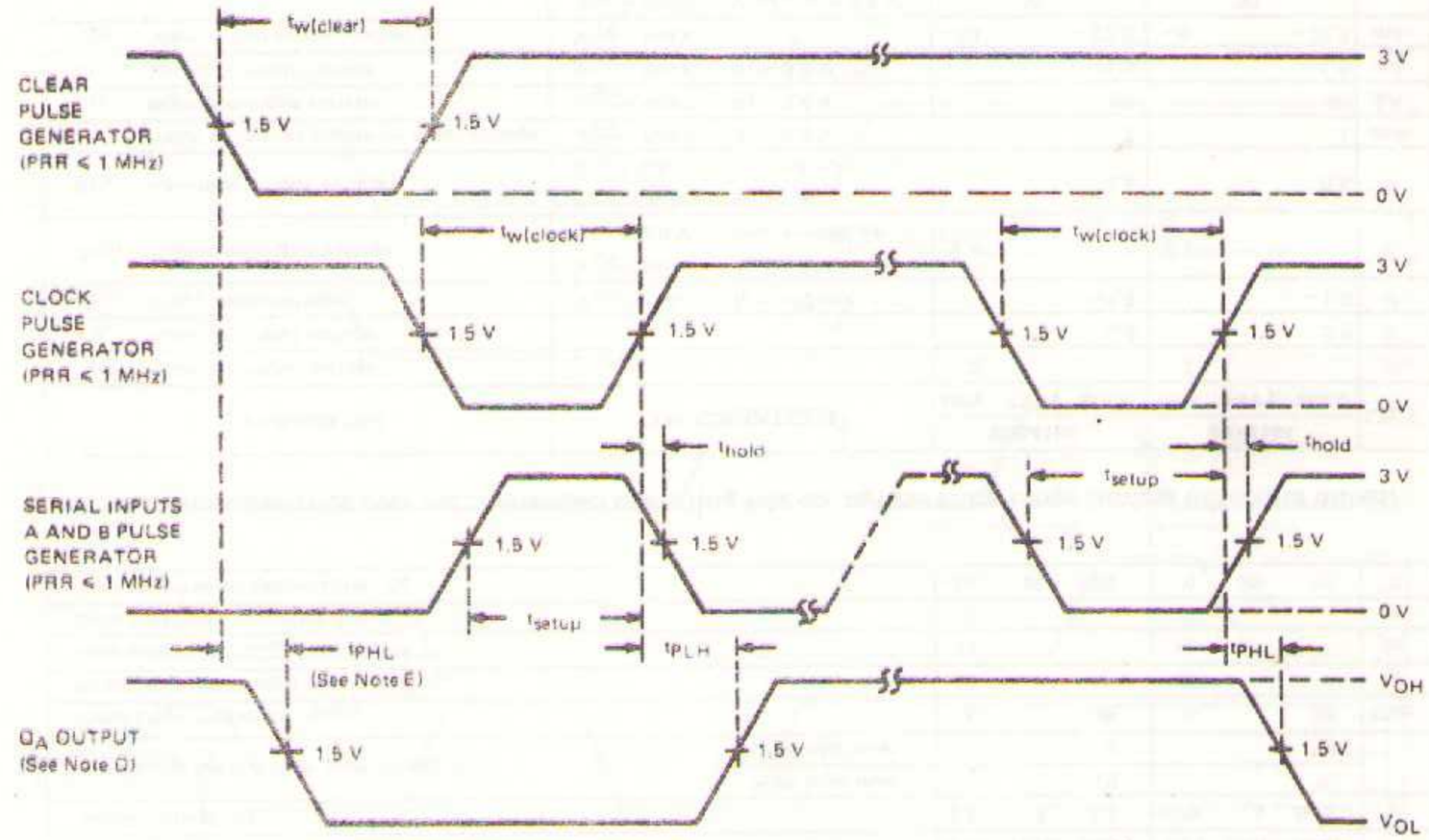
functional block diagram



PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



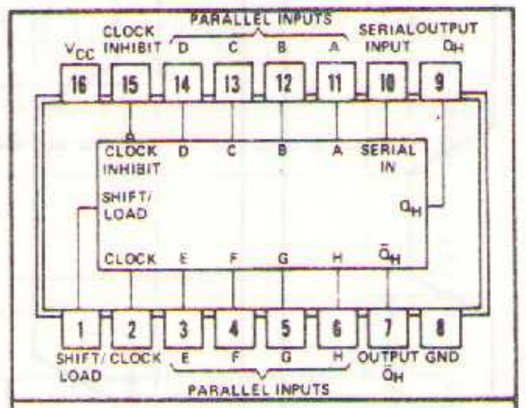
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, duty cycle ≤ 50%, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Q_A output is illustrated. Relationship of serial input A and B data to other Q outputs is illustrated in the typical shift sequence.
E. Outputs are set to the high level prior to the measurement of t_{PHL} from the clear input.

FIGURE 1—SWITCHING TIMES

- Typical Maximum Input Clock Frequency . . . 26 MHz
- Complementary Outputs
- Direct Overriding Load (Data) I[illegible]ts
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: see description

†Pin assignments for these circuits are the same for all packages.

description

The SN54165 and SN74165 are 8-bit serial shift registers which shift the data to the right when clocked. Parallel-in access to each stage is made available by eight individual direct data inputs which are enabled by a low level at the shift/load input. These registers also feature gated clock inputs and complementary outputs from the eighth bit.

Clocking is accomplished through a 2-input positive-NOR gate, permitting one input to be used as a clock-inhibit function. Holding either of the clock inputs high inhibits clocking, and holding either clock input low with the load input high enables the other clock input. The clock-inhibit input should be changed to the high level only while the clock input is high. Parallel loading is inhibited as long as the load input is high. When taken low, data at the parallel inputs are loaded directly into the reg ·ter independently of the state of the clock.

All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design. Power dissipation is typically 210 milliwatts and maximum input clock frequency is typically 26 megahertz. The SN54165 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74165 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54165 Circuits	−55°C to 125°C
SN74165 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values, except interemitter voltage, are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to the shift/load input in conjunction with the clock or clock-inhibit inputs.

recommended operating conditions

		SN54165			SN74165			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		15			15			ns
Clock-enable setup time, t_{setup} (see Figure 1)		30			30			ns
Parallel input setup time, t_{setup} (see Figure 1)		10			10			ns
Serial input setup time, t_{setup} (see Figure 2)		20			20			ns
Shift setup time, t_{setup} (see Figure 2)		45			45			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54165 MIN	SN54165 TYP‡	SN54165 MAX	SN74165 MIN	SN74165 TYP‡	SN74165 MAX	UNIT
V_{IH} High-level input voltage			2			2			V
V_{IL} Low-level input voltage					0.8			0.8	V
V_I Input clamp voltage		V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH} High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL} Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH} High-level input current	Load input	V_{CC} = MAX, V_I = 2.4 V			80			80	μA
	Other inputs				40			40	
I_{IL} Low-level input current	Load input	V_{CC} = MAX, V_I = 0.4 V			−3.2			−3.2	mA
	Other inputs				−1.6			−1.6	
I_{OS} Short-circuit output current§		V_{CC} = MAX	−20		−55	−18		−55	mA
I_{CC} Supply current		V_{CC} = MAX, See Note 3		42	63		42	63	mA

NOTE 3: With the outputs open, clock inhibit and shift/load at 4.5 V, and a clock pulse applied to the clock input, I_{CC} is measured first with the parallel inputs at 4.5 V, then with the parallel inputs grounded.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

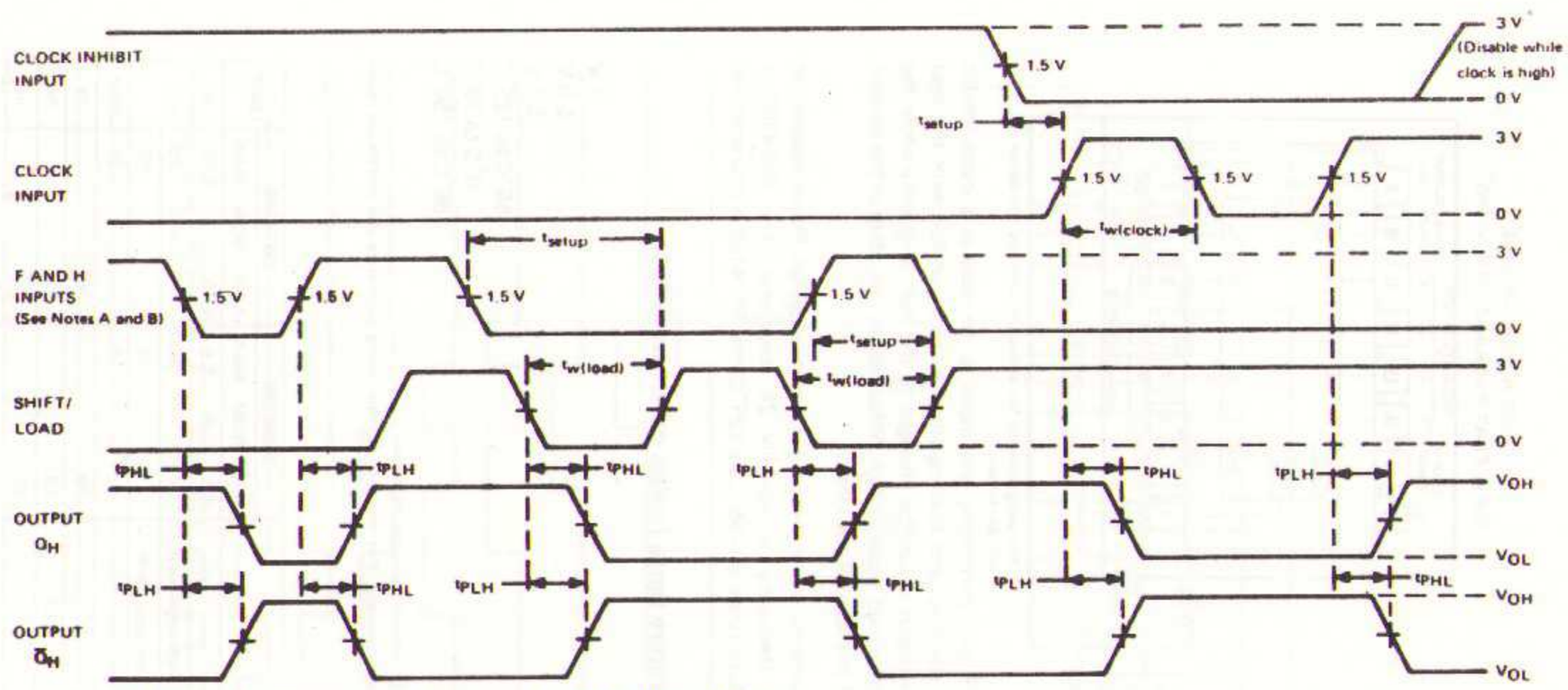
PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See figures 1 thru 3	20	26		MHz
t_{PLH}	Load	Any			21	31	ns
t_{PHL}					27	40	
t_{PLH}	Clock	Any			16	24	ns
t_{PHL}					21	31	
t_{PLH}	H	Q_H			11	17	ns
t_{PHL}					24	36	
t_{PLH}	H	$\bar{Q}_H$			18	27	ns
t_{PHL}					18	27	

¶f_{max} ≡ Maximum input count frequency
t_{PLH} ≡ Propagation delay time, low-to-high-level output
t_{PHL} ≡ Propagation delay time, high-to-low-level output

VAN DAM ELEKTRONICA

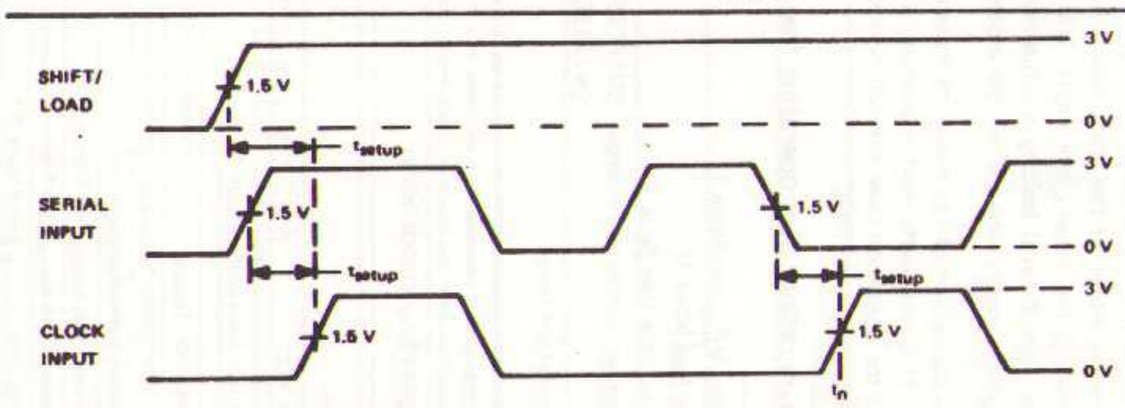
PRINTSERVICE

Sinds het betrekken van ons bedrijfspand aan de Spoorsingel te Rotterdam ontplooiden wij ook nieuwe activiteiten op het gebied van printservice. Voor het vervaardigen van kleine of grote series prints is nu Van Dam Elektronica ook in te schakelen tegen een concurrerende prijs en levertijd. Voor nadere informaties verwijzen wij U naar een achter in deze documentatie opgenomen aankondiging.



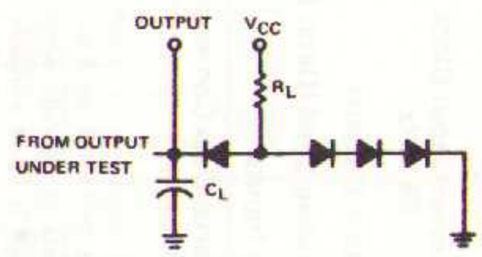
NOTES: A. The remaining six data inputs and the serial input are low.
B. Prior to test, high-level data is loaded into H input.
C. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\ \Omega$. When testing f_{max}, vary clock PRR.

FIGURE 1—VOLTAGE WAVEFORMS



NOTES: A. The eight data inputs and the clock-inhibit input are low. Results are monitored at output Q_H at t_{n+7}.
B. The input pulse generators have the following characteristics: $t_r \leq 10$ ns, $t_f \leq 10$ ns, PRR $\leq$ 1 MHz, duty cycle $\leq$ 50%, $Z_{out} \approx 50\ \Omega$.

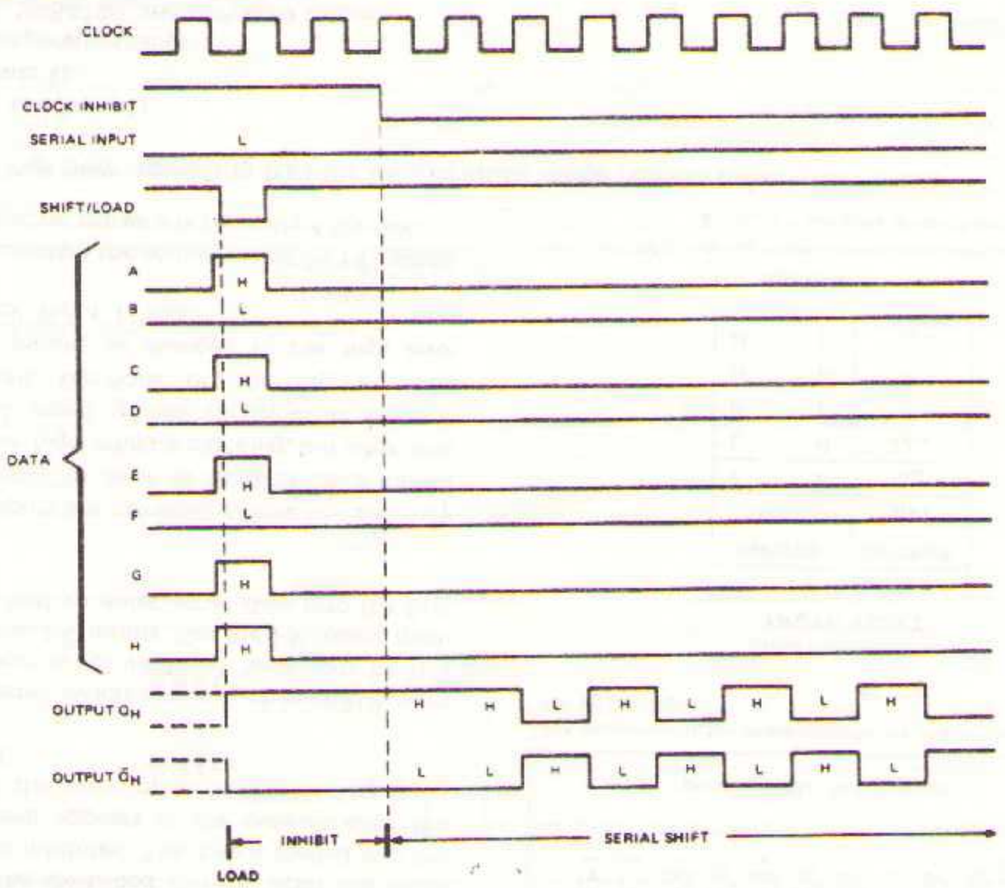
FIGURE 2—VOLTAGE WAVEFORMS



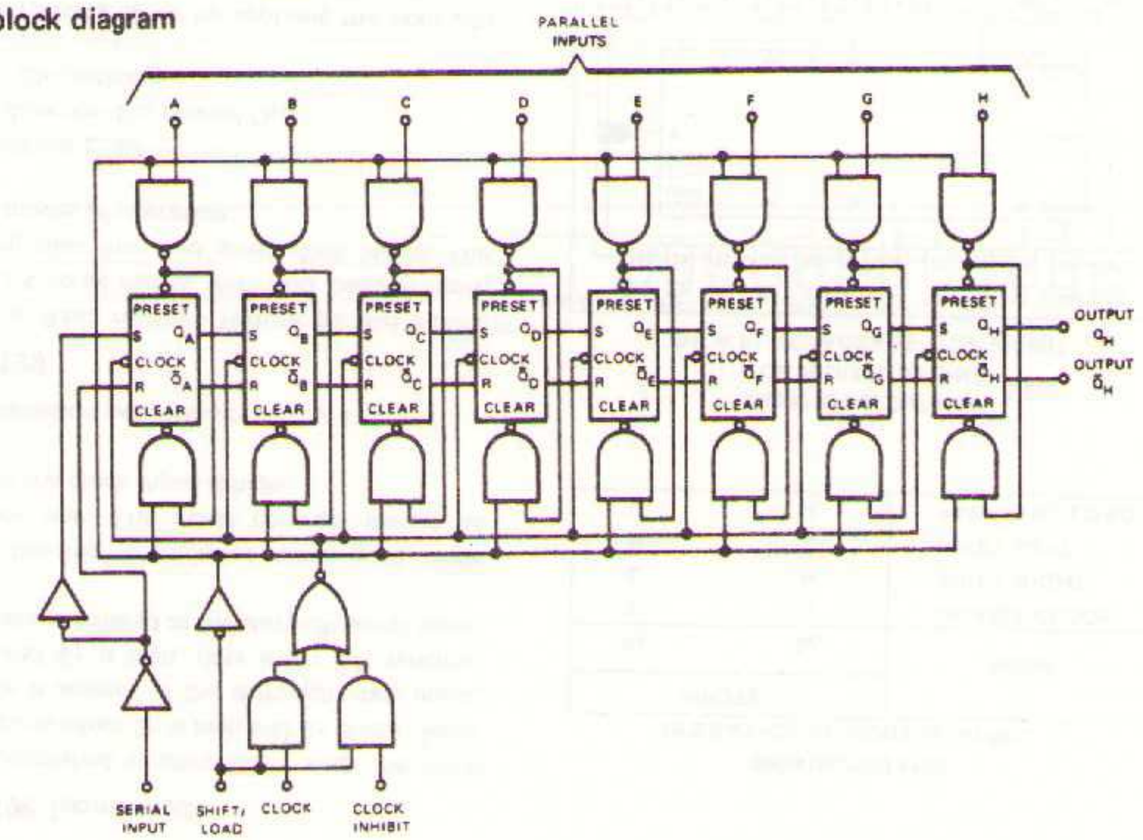
NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are IN3064.

FIGURE 3—LOAD CIRCUIT FOR SWITCHING TESTS

typical shift, load, and inhibit sequences



functional block diagram



description

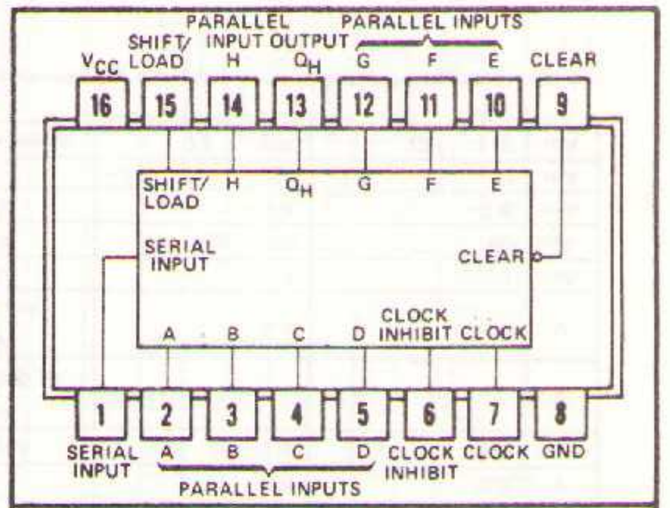
These 8-bit shift registers are compatible with most other TTL, DTL, and MSI logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 35 megahertz and power dissipation is typically 360 mW.

All Series 54 devices are characterized for operation over the full military temperature range of −55°C to 125°C; all Series 74 devices are characterized for operation from 0°C to 70°C.

SN54166 and SN74166

These parallel-in or serial-in, serial-out shift registers have a complexity of 77 equivalent gates on a monolithic chip. They feature gated clock inputs and an overriding clear input. The parallel-in or serial-in modes are established by the shift/load input. When high, this input enables the serial data input and couples the eight flip-flops for serial shifting with each clock pulse. When low, the parallel (broadside) data inputs are enabled and synchronous loading occurs on the next clock pulse. During parallel loading, serial data flow is inhibited. Clocking is accomplished on the low-to-high-level edge of the clock pulse through a two-input positive NOR gate permitting one input to be used as a clock-enable or clock-inhibit function. Holding either of the clock inputs high inhibits clocking; holding either low enables the other clock input. This, of course, allows the system clock to be free-running and the register can be stopped on command with the gate input. The clock-inhibit input should be changed to the high level only while the clock input is high. A buffered, direct clear input overrides all other inputs, including the clock and sets all flip-flops to zero. Average power dissipation per gate is typically 4.7 mW.

SN54166 and SN74166
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

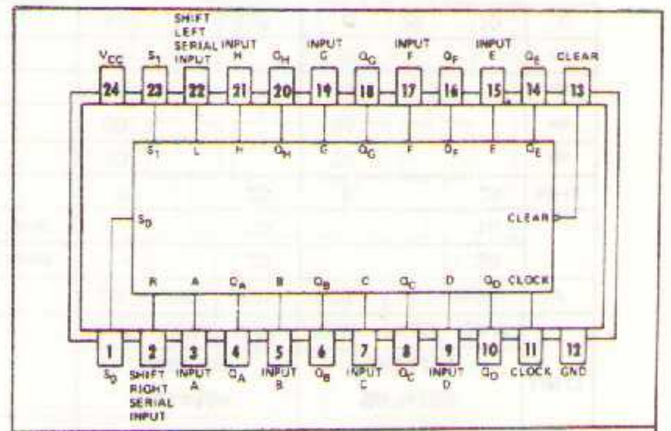
SN54198 and SN74198

The bidirectional registers are designed to incorporate virtually all of the features a system designer may want in a shift register. These circuits contains 87 equivalent gates and feature parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

Parallel (Broadside) Load
Shift Right (In the direction Q_A toward Q_H)
Shift Left (In the direction Q_H toward Q_A)
Inhibit Clock (Do nothing)

Synchronous parallel loading is accomplished by applying the eight bits of data and taking both mode control inputs, S_0 and S_1, high. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

SN54198 and SN74198
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See truth table for mode control (S_0, S_1)

†Pin assignments for these circuits are the same for all packages.

SN54198 and SN74198 (continued)

Shift right is accomplished synchronously with the rising edge of the clock pulse when S_0 is high and S_1 is low. Serial data for this mode is entered at the shift-right data input. When S_0 is low and S_1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the flip-flop is inhibited when both mode control inputs are low. The mode controls should be changed only while the clock input is high.

Average power dissipation per gate is typically 4.15 mW.

SN54198/SN74198
OPERATION OF MODE CONTROL

INPUTS S_1	INPUTS S_0	MODE
L	L	INHIBIT CLOCK
L	H	SHIFT RIGHT
H	L	SHIFT LEFT
H	H	PARALLEL LOAD

SN54199 and SN74199

These synchronous 8-bit registers feature parallel inputs, parallel outputs, J-K serial inputs, shift/load control input, a direct overriding clear line, and gated clock inputs. The register has three modes of operation:

Parallel (Broadside) Load
Shift (In the direction Q_A toward Q_H)
Inhibit Clock (Do nothing)

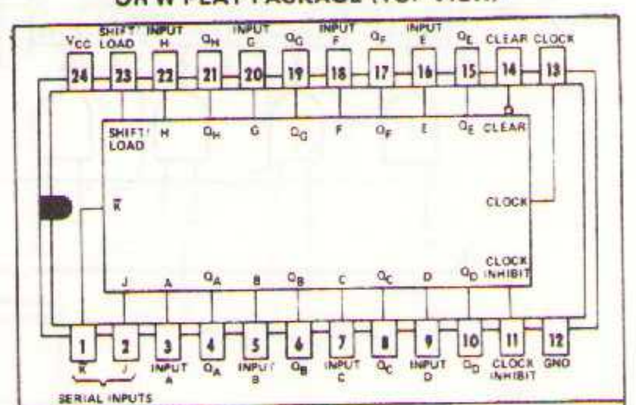
Parallel loading is accomplished by applying the eight bits of data and taking the shift/load control input low when the clock input is not inhibited. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when shift/load is high and the clock input is not inhibited. Serial data for this mode is entered at the J-$\overline{K}$ inputs. See the J-$\overline{K}$ inputs truth table for states required to enter serial data into the first flip-flop.

Both of the clock inputs are identical in function and may be used interchangeably to serve as clock or clock-inhibit inputs. Holding either high inhibits clocking, but when one is held low, a clock input applied to the other input is passed to the eight flip-flops of the register. The clock-inhibit input should be changed to the high level only while the clock input is high.

These shift registers contain the equivalent of 79 TTL gates. Average power dissipation per gate is typically 4.55 mW.

SN54199 and SN74199
J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



positive logic: See description

†Pin assignments for these circuits are the same for all packages.

SN54199/SN74199
TRUTH TABLE
J-$\overline{K}$ INPUTS

INPUTS at t_n, J	K̄	OUTPUT t_{n+1} Q_A
L	H	Q_{An}
L	L	L
H	H	H
H	L	$\overline{Q}_{An}$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range:
SN54166, SN54198, and SN54199 Circuits . . . . . −55°C to 125°C
SN74166, SN74198, and SN74199 Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54166 SN54198 SN54199 MIN	NOM	MAX	SN74166 SN74198 SN74199 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input count frequency, f_{count}		0		25	0		25	MHz
Width of clock or clear pulse, t_w (see Figure 1)		20			20			ns
Mode-control setup time, t_{setup}		30			30			ns
Data setup time, t_{setup} (see Figure 1)		20			20			ns
Hold time at any input, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54166 SN54198 SN54199 MIN	TYP‡	MAX	SN74166 SN74198 SN74199 MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MAX, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−57	−18		−57	mA
I_{CC}	Supply current	V_{CC} = MAX, See Table Below		72	104		72	116	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

TEST CONDITIONS FOR I_{CC}
(ALL OUTPUTS ARE OPEN.)

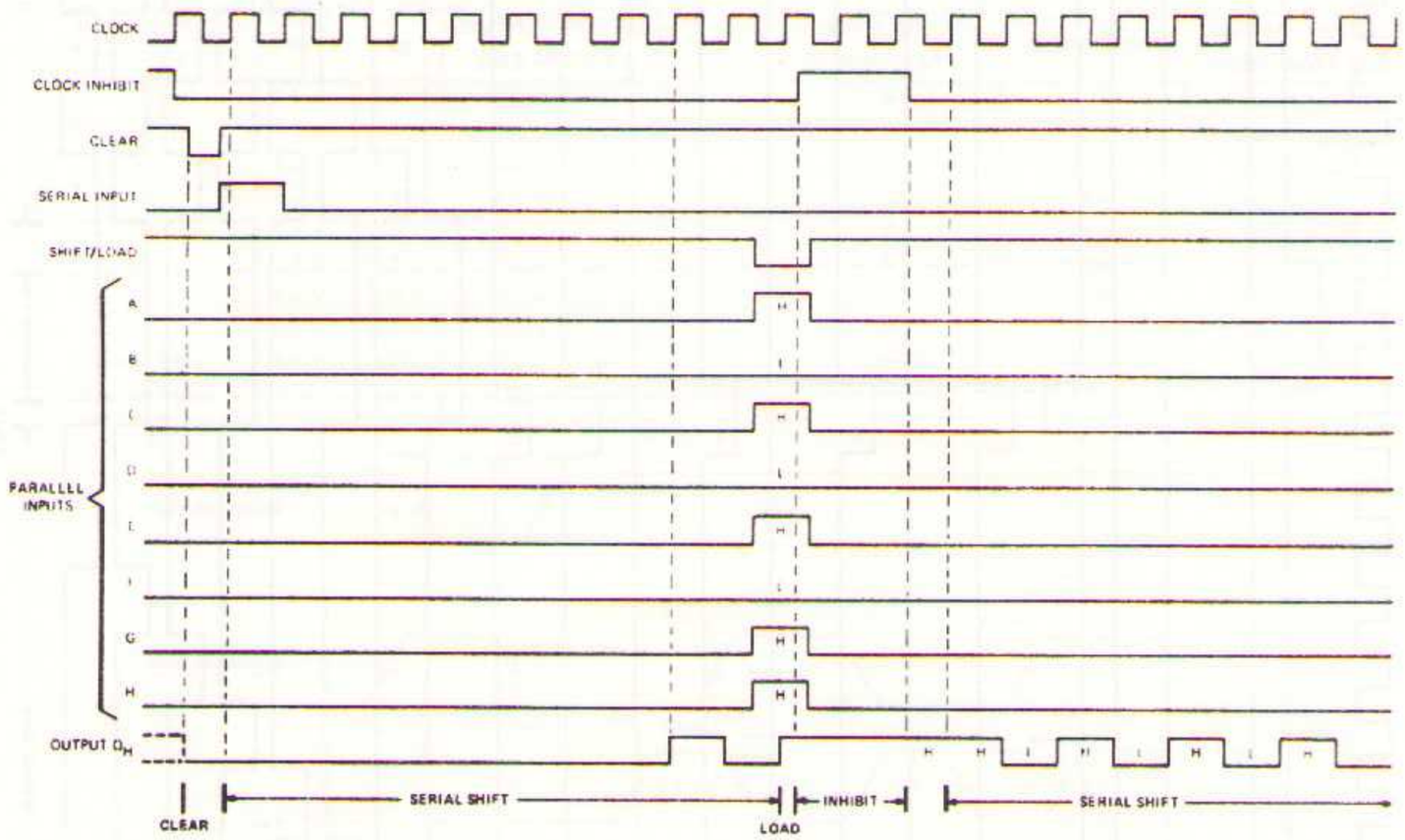
TYPE	APPLY 4.5 V	FIRST GROUND, THEN APPLY 4.5 V	GROUND
SN54166, SN74166	Serial Input	Clock	All other inputs
SN54198, SN74198	Serial Input, S_0, S_1	Clock	Clear, Inputs A thru H
SN54199, SN74199	J, K̄, Inputs A thru H	Clock	Clock Inhibit, Clear, Shift/Load

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input count frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	35		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			23	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		8	20	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		8	17	26	ns

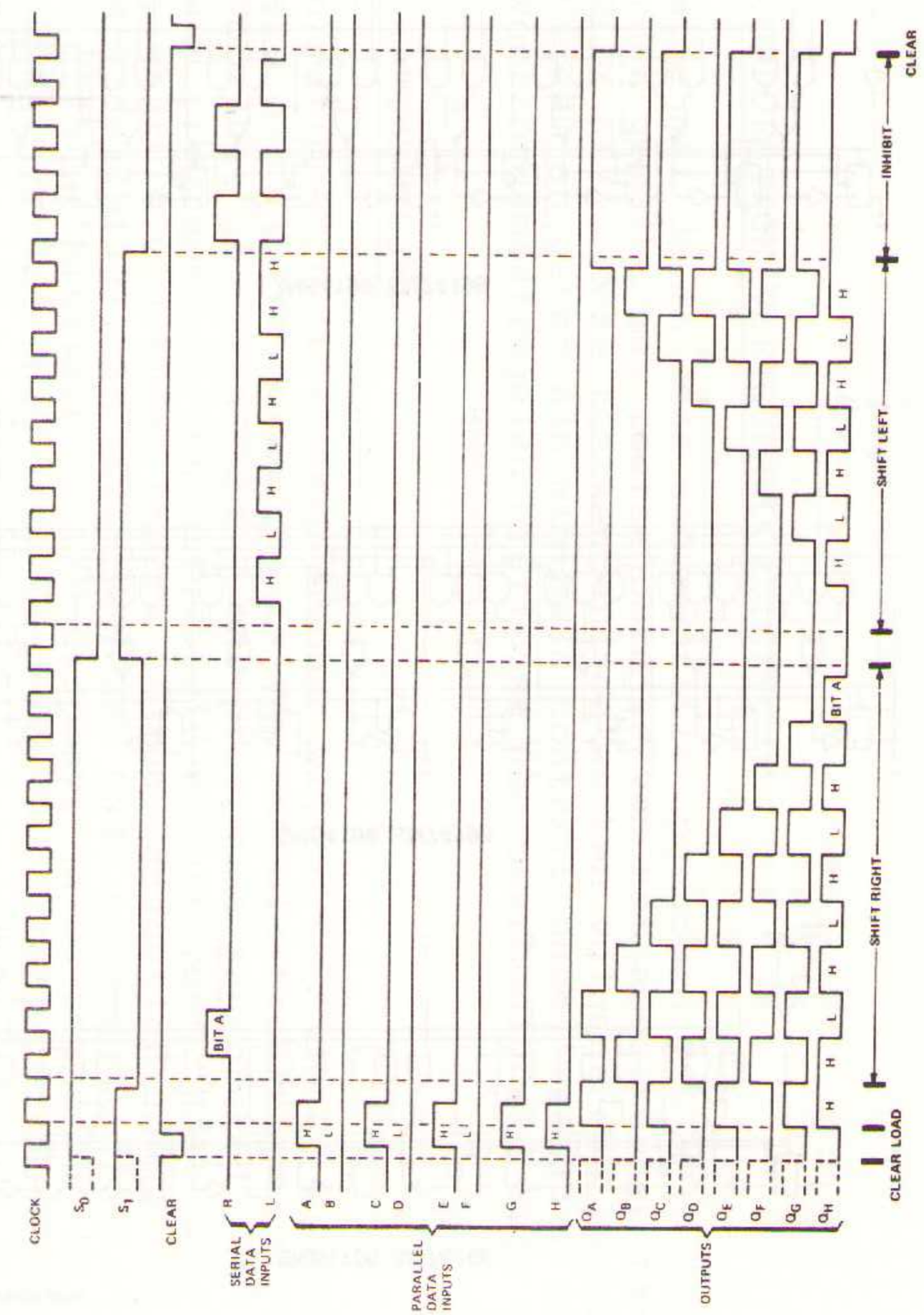
SN54166, SN74166

typical clear, shift, load, inhibit, and shift sequences



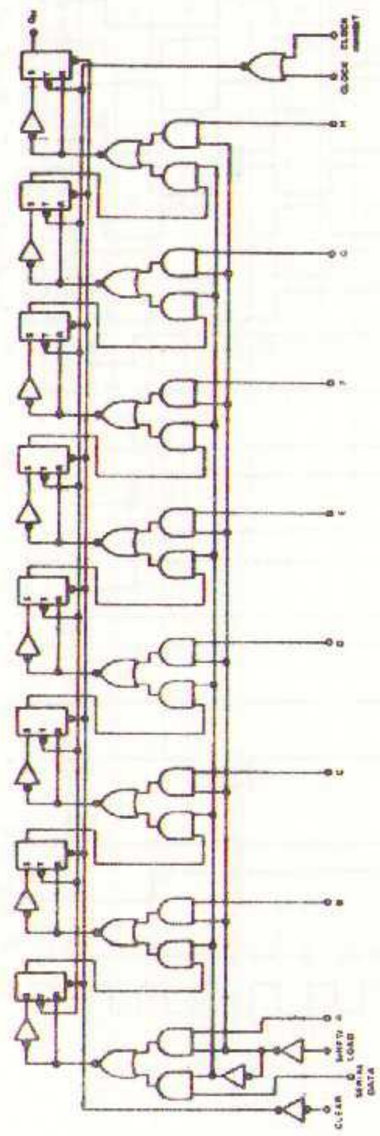
SN54198, SN74198

typical clear, load, right-shift, left-shift, inhibit, and clear sequences

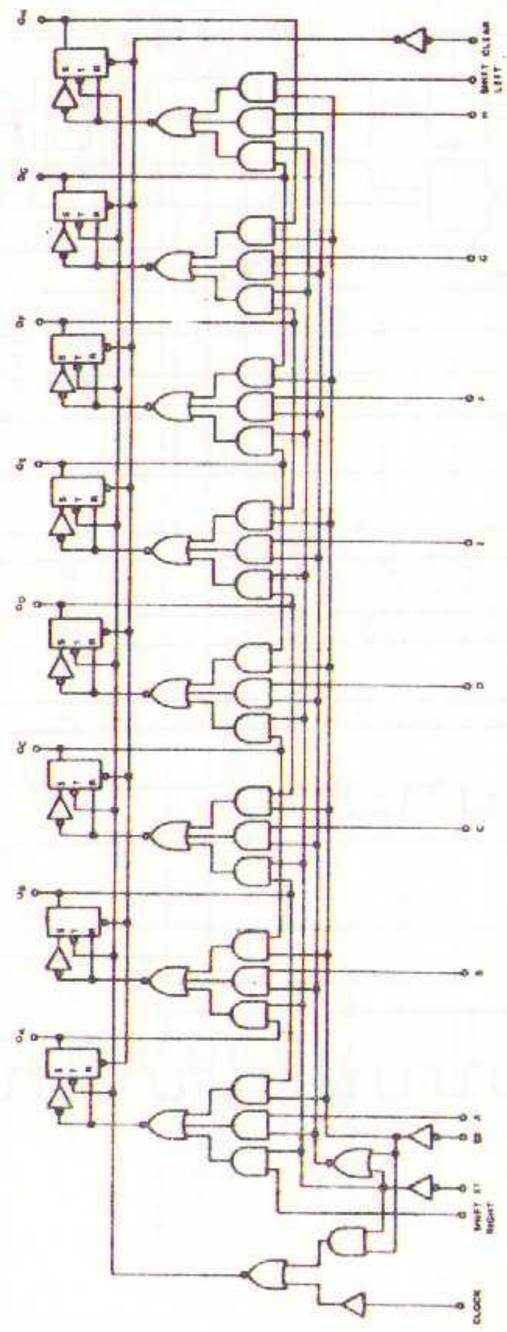


functional block diagrams

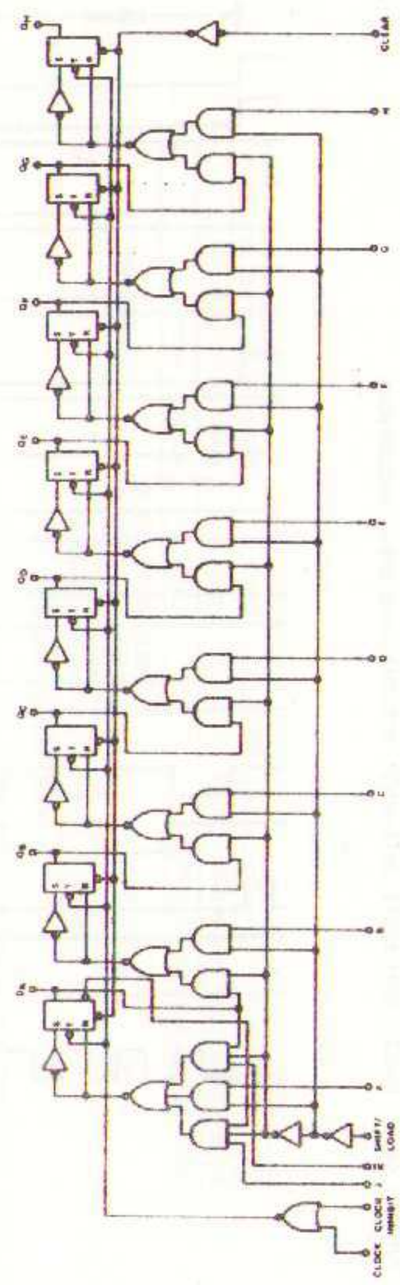
SN54166, SN74166



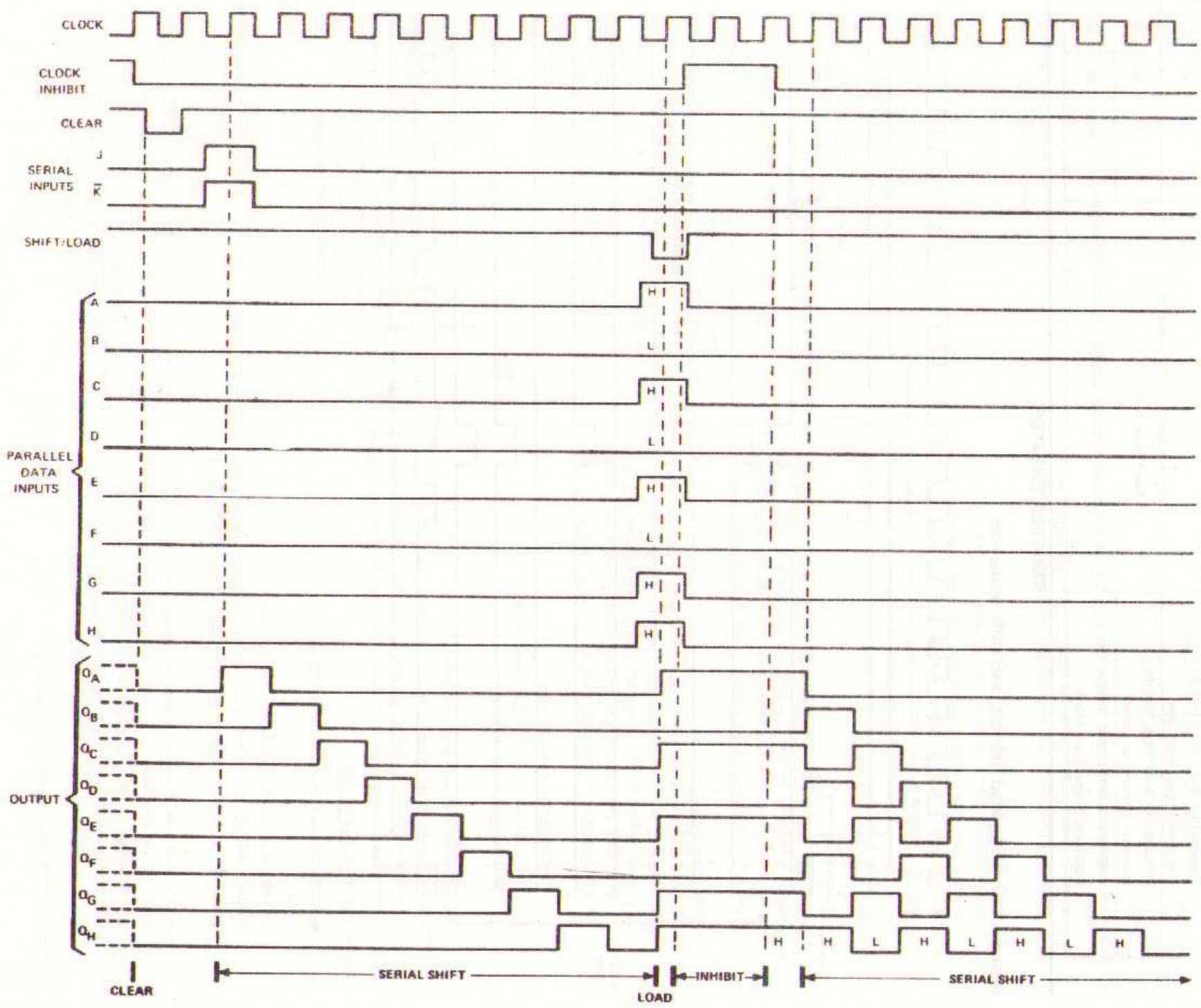
SN54198, SN74198



SN54199, SN74199



typical clear, shift, load, and inhibit sequences



FLEX KEY CORPORATION VERTEGENWOORDIGING

In kombinatie met de in deze documentatie opgenomen TTL IC's kan ideaal worden gewerkt met toetsenbordjes van het amerikaanse fabrikaat 'FLEX KEY'. Deze toetsenbordjes werken volgens een revolutionair systeem en geven een minimale kontaktbounce, waardoor zeer speciale voorzorgsmaatregelen hiertegen een overbodigheid zijn geworden.

CIJFERINDIKATIEBUISJES

Om de informatie erin te stoppen hebben wij verschillende produkten, om deze met TTL te verwerken is Van Dam Elektronica uw adres doch ook voor het uitlezen kunt U ons programma aanspreken. In het voorraad programma is een uitgebreid assortiment indicators opgenomen, waaruit wij onder andere noemen: gasontladingsbuizen ZM1000, ZM1020, ZM1021, ZM 1022, ZM1024, GN4P en 7-segment displays type 3015F ('Minitron'), LED-displays en DG-serie van het fabrikaat Ise International Ltd. (een Van Dam Elektronica vertegenwoordiging).

GEGEVENS OVER BOVENSTAANDE PROGRAMMA's WORDEN DIT JAAR GEPUBLICEERD IN DE TECHNISCHE DOCUMENTATIE OF VOOR BELANGSTELLENDEN OP AANVRAAG VERSTREKT; RICHT UW AANVRAAG AAN VAN DAM ELEKTRONICA, POSTBUS 450, ROTTERDAM-3004, TELEFOON: 010-670022, TELEX 25336.

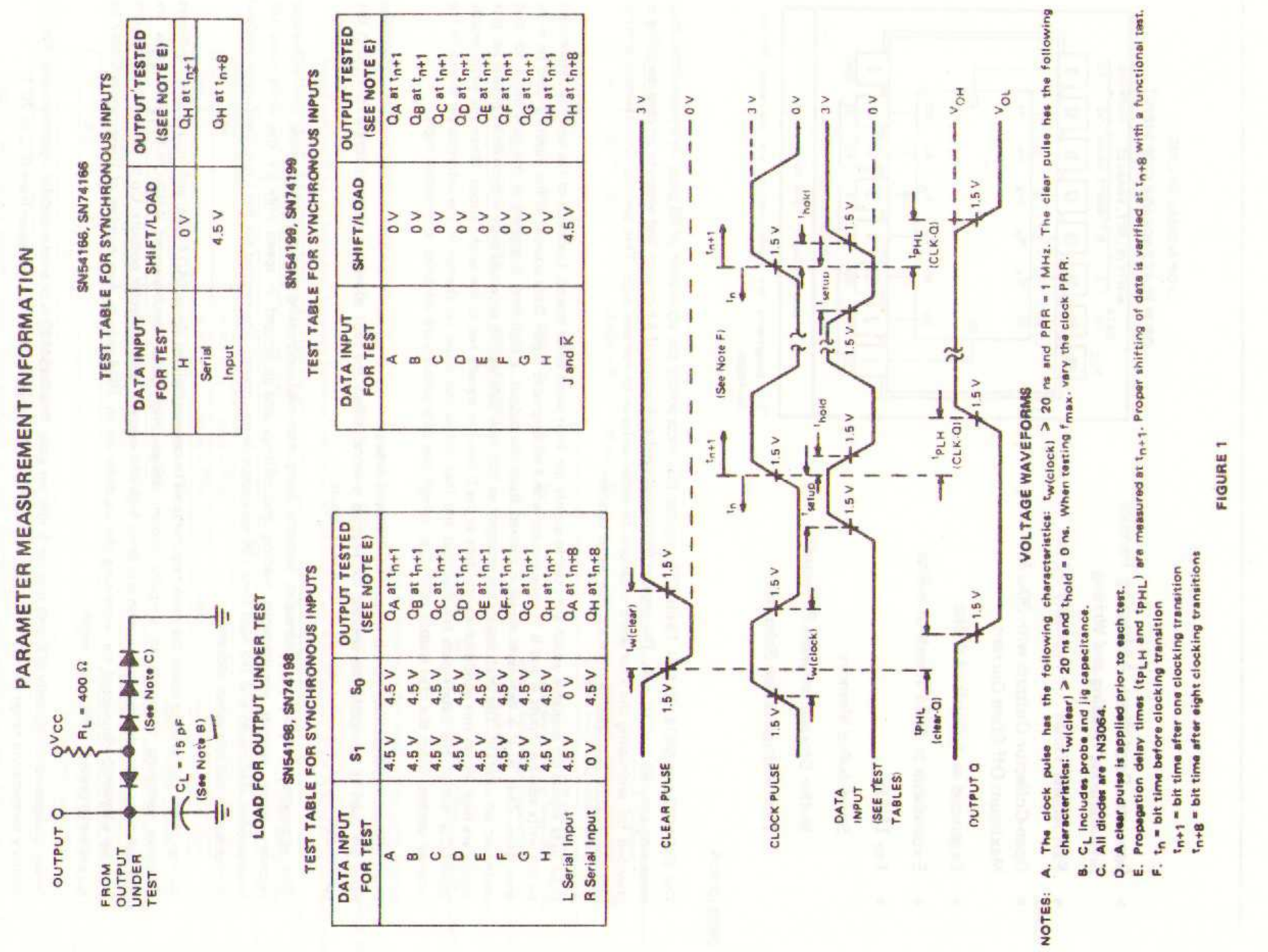


FIGURE 1

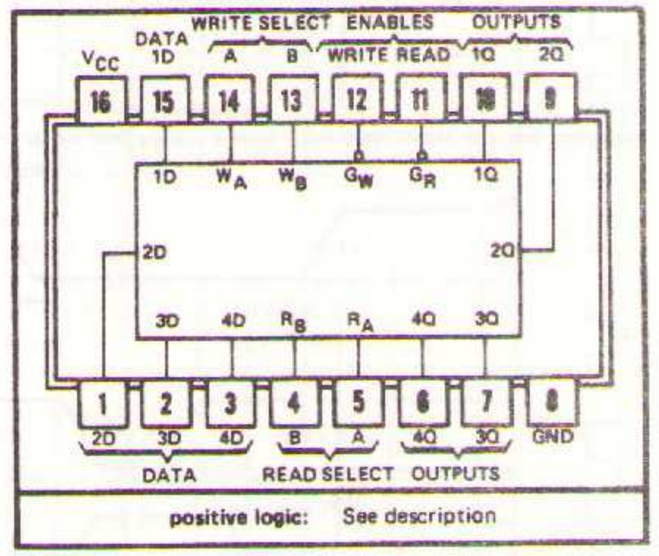
- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times . . . Typically 20 ns
- Open-Collector Outputs with 30-μA Maximum Off-State Current
- Organized as 4 Words of 4 Bits
- Expandable to 1024 Words of n-Bits
- For Use as:

  Scratch-Pad Memory

  Buffer Storage between Processors

  Fast Multiplication Schemes

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assigments for these circuits are the same for all packages.

description

The SN54170 and SN74170 MSI 16-bit TTL register files incorporate the equivalent of 98 gates on a monolithic chip measuring only 90 by 110 mils. The register file is organized as 4 words of 4 bits each and separate on-chip decoding is provided for addressing the four word locations to either write-in or retrieve data. This permits simultaneous writing into one location and reading from another word location.

Four data inputs are available which are used to supply the 4-bit word to be stored. Location of the word is determined by the write address inputs A and B in conjunction with a write-enable signal. Data applied at the inputs should be in its true form. That is, if a high-level signal is desired from the output, a high-level is applied at the data input for that particular bit location. The latch inputs are arranged so that new data will be accepted only if both internal address gate inputs are high. When this condition exists, data at the D input is transferred to the latch output. When the write enable input, G_W is high, the data inputs are inhibited and their states can cause no change in the information stored in the internal latches. When the read enable input, G_R, is high, the data outputs are inhibited and remain high.

The individual address lines permit direct acquisition of data stored in any four of the latches. Four individual decoding gates are used to complete the address for reading a word. When the read address is made in conjunction with the read-enable signal, the word appears at the four outputs.

This arrangement—data-entry addressing separate from data-read addressing and individual sense line—eliminates recovery times, permits simultaneous reading and writing, and is limited in speed only by the write time (45 nanoseconds maximum) and the read time (35 nanoseconds maximum). The register file has a non-destructive readout in that data is not lost when addressed.

All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input-clamping diodes minimize switching transients to simplify system design. High-speed, double-ended AND-OR-INVERT gates are employed for the read-address function and drive high-sink-current, open-collector outputs. Up to 256 of these outputs may be wire-AND connected for increasing the capacity up to 1024 words. Any number of these registers may be paralleled to provide n-bit word length.

Power dissipation is typically 500 mW total or 5 mW per gate. The SN54170 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74170 is characterized for operation from 0°C to 70°C.

logic

WRITE FUNCTION TABLE (SEE NOTES A, B, AND C)

WRITE INPUTS			WORD			
W_B	W_A	G_W	0	1	2	3
L	L	L	Q = D	Q_n	Q_n	Q_n
L	H	L	Q_n	Q = D	Q_n	Q_n
H	L	L	Q_n	Q_n	Q = D	Q_n
H	H	L	Q_n	Q_n	Q_n	Q = D
X	X	H	Q_n	Q_n	Q_n	Q_n

READ FUNCTION TABLE (SEE NOTES A AND D)

READ INPUTS			OUTPUTS			
R_B	R_A	G_R	1Q	2Q	3Q	4Q
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

NOTES: A. H = high level, L = low level, X = irrelevant
B. (Q = D) = The four selected internal flip-flop outputs will assume the states applied to the four external data inputs.
C. Q_n = No change.
D. W0B1 = The first bit of word 0, etc.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Output voltage (see Notes 1 and 2)		5.5 V
Operating free-air temperature range:	SN54170J Circuits	−55°C to 125°C
	SN74170J, N Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the maximum voltage which should be applied to any output when it is in the off state.

recommended operating conditions

		SN54170			SN74170			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}				16			16	mA
Width of write-enable or read-enable pulse, t_w		25			25			ns
Setup times, high- or low-level data (see Note 3 and Figure 1)	data input with respect to write enable, $t_{setup(D)}$	10			10			ns
	write select with respect to write enable, $t_{setup(W)}$	15			15			ns
	read select with respect to read enable, $t_{setup(R)}$	5			5			ns
Hold times, high- or low-level data (see Note 4 and Figure 1)	data input with respect to write enable, $t_{hold(D)}$	0			0			ns
	write select with respect to write enable, $t_{hold(W)}$	5			5			ns
	read select with respect to read enable, $t_{hold(R)}$	5			5			ns
Latch time for new data, t_{latch} (see Note 5)		25			25			ns
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

NOTES: 3. Setup time is the interval immediately preceding the negative-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the positive-going edge of the enable pulse during which interval the data or address to be recognized must be maintained at the input to ensure its continued recognition.
5. Latch time is the time required for the internal output of the latch to assume the state of new data. See Figure 1. This is important only when attempting to read from a location immediately after that location has received new data.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN,	V_O = 5.5 V			30	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, I_{OL} = 16 mA	V_{IL} = 0.8 V,			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V			−1.6	mA
I_{CC}	Supply current	V_{CC} = MAX, see Note 6	SN54170		127‡	140	mA
			SN74170		127‡	150	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

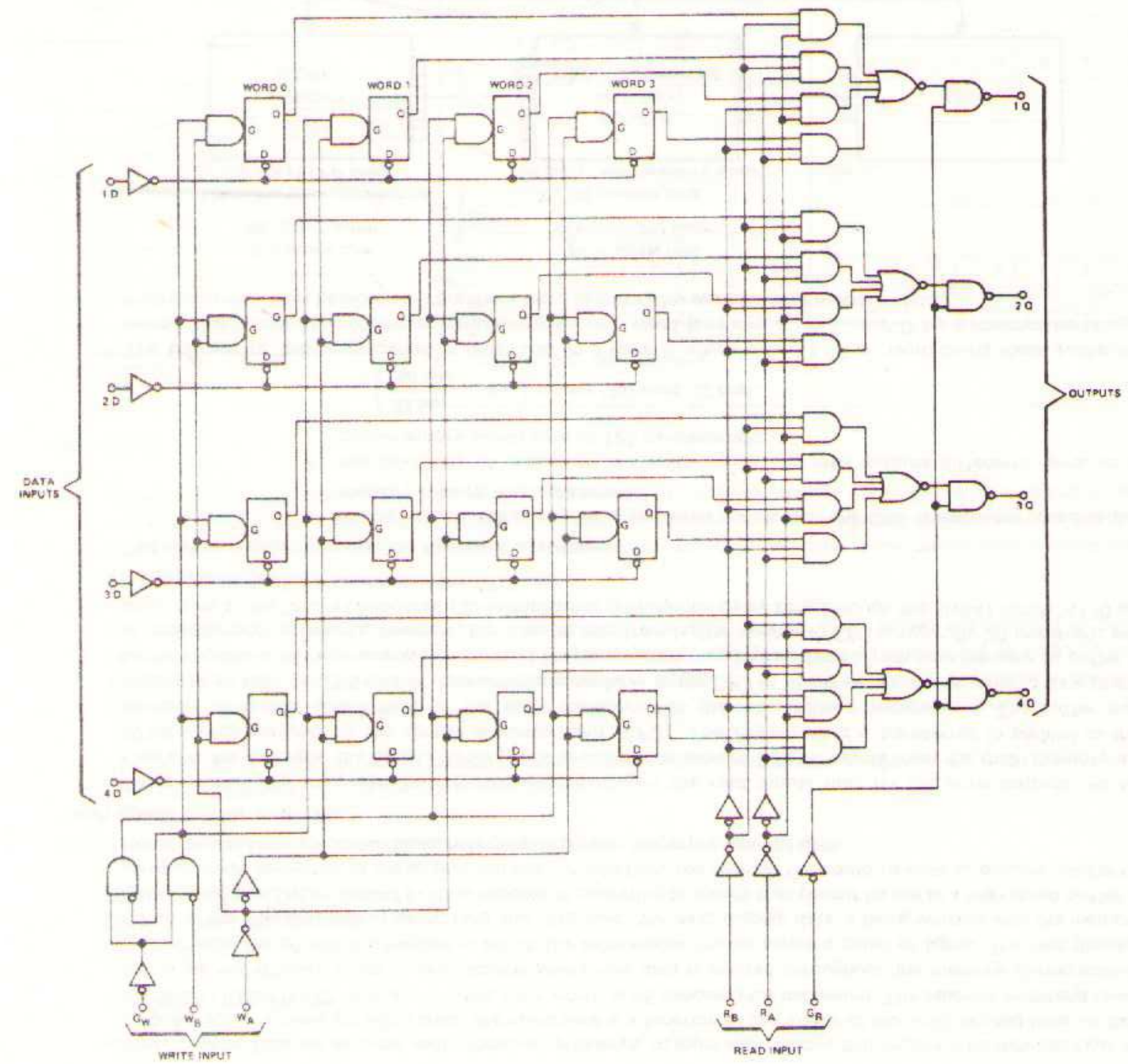
‡Typical power dissipation shown is an average for 50% duty cycle at V_{CC} = 5 V, T_A = 25°C.

NOTE 6: Maximum I_{CC} is guaranteed for the following worst-case conditions. 4.5 V is applied to all data inputs and both enable inputs, all address inputs are grounded, and all outputs are open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

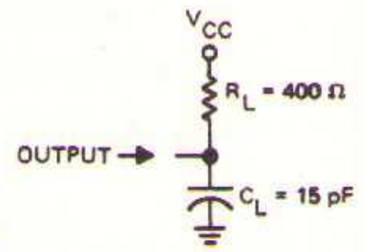
PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		10	15	ns
t_{PHL}	Propagation delay time, high-to-low-level output, from read enable to any Q	C_L = 15 pF,	R_L = 400 Ω		20	30	ns

functional block diagram



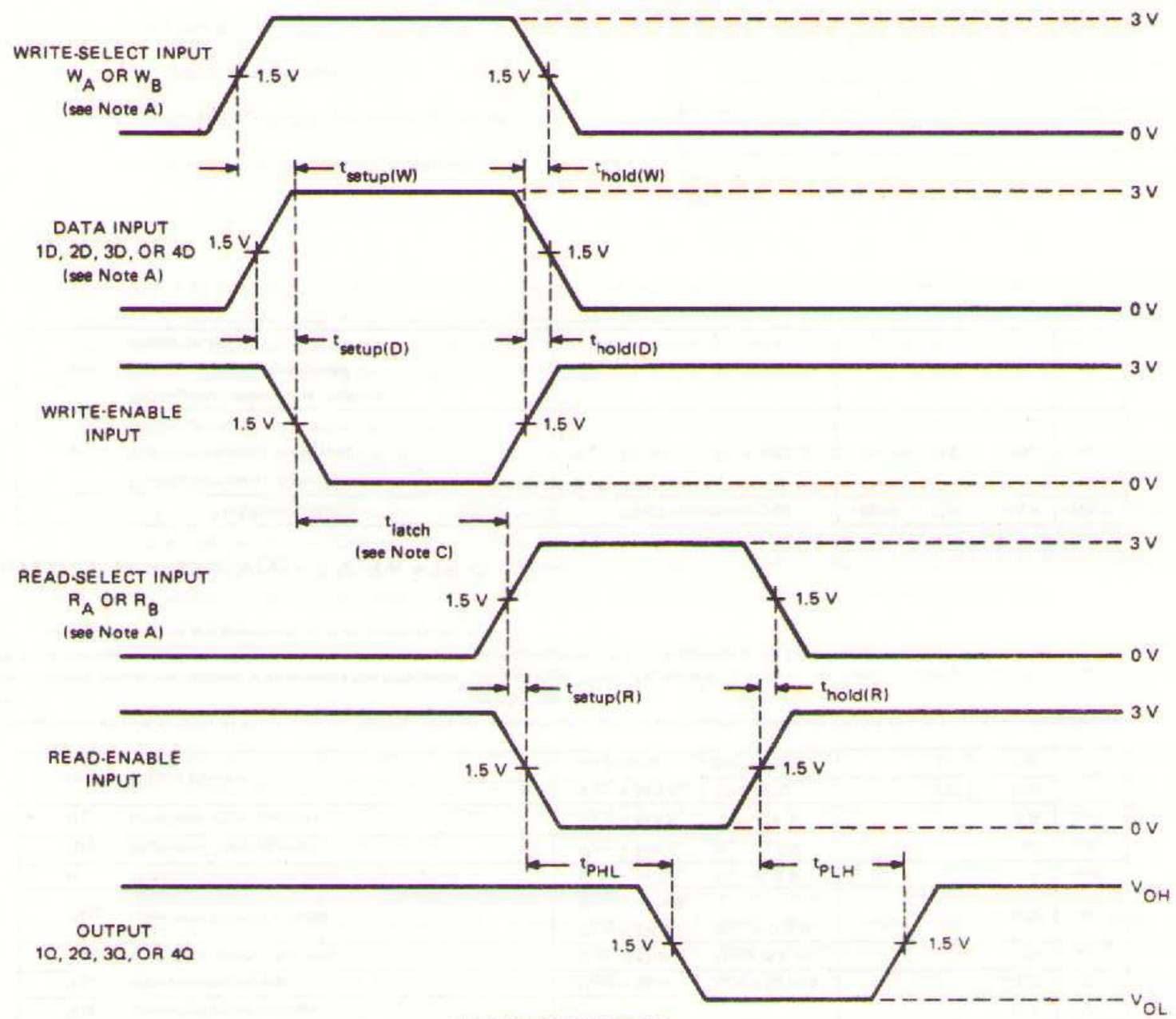
PARAMETER MEASUREMENT INFORMATION

switching characteristics



NOTE: C_L includes probe and jig capacitance.

LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. High-level inputs are illustrated; however, low-level setup and hold times are the same.
B. Waveforms are supplied by generators with the following characteristics: PRR ≤ 1 MHz, Z_{out} ≈ 50 Ω, duty cycle ≤ 50%, t_r ≤ 10 ns, t_f = 10 ns.
C. This applies only when reading from a location immediately after that location has received new data.

FIGURE 1–SWITCHING TIMES

TYPICAL APPLICATION DATA

general

These register files may be cascaded to form n-bit registers with capacities of 1024 words. Word capacity is increased by wire-AND connecting the four outputs of a number of register files (up to 256). One write-select and one read-select register is required for all the paralleled files.

For increased word length (number of bits), a number of files may be selected and enabled simultaneously to provide the desired word length. This scheme is compatible for using parallel files to provide more words also. All inputs and outputs, except the write-enable and read-enable lines, are paralleled to add word capacity. The enable lines are separate for each word.

These register files can be used with improved efficiency in most applications that require a scratch-pad-type memory. Because recovery times are eliminated, the cycle time is a function of the longer of the write or read time. In the case of the SN54170/SN74170, this is the write time which is 45 nanoseconds maximum. The separate write and read address inputs permit efficient usage in applications where new data is entered throughout the memory during each cycle. A familiar example of this is a display in which the information moves across a panel of lights. The first display data is stored in the file, and as it is being read and displayed, the next display data is being written into the memory. More realistically, the SN54170/SN74170 is capable of operating at speeds that permit its use as a high-speed buffer memory between main memories or peripheral stations. In addition, the register file could be used to acquire tabular data, as a complete table or on a partial basis, recycling to present the entire bank of data.

high-speed buffer memory

These register files may also be organized differently on the read inputs than on the write outputs. As shown in Figure A, for example, the SN54170/SN74170 is utilized to acquire 256-bit words from the main memory and make 32-bit words available to the central processor unit (CPU). The 256-bit word is transferred in parallel to the buffer memory. A typical access time to the main memory is in the order of one microsecond. The buffer memory is organized so that the 256 bits of data are made available to the CPU in 32-bit words. Access time to data stored in the buffer register is 35 nanoseconds. In terms of frequency, data may be transferred from core memory to buffer memory at typically one megahertz; however, the transfer rate from buffer register to CPU is typically 20 megahertz when data setup time at the CPU is considered (30 nanoseconds propagation delay time through the SN54170/SN74170 and 10 to 20 nanoseconds data setup time in the CPU).

This buffer memory provides the following advantages:

- ability to simultaneously read and write means that the CPU is not interrupted as the buffer memory is being re-programmed
- the flexibility of organizing the write inputs and read outputs differently gives an effective main-memory access time of 125 nanoseconds:

$$\left(\frac{32\text{ bits}}{256\text{ bits}} \times 1\ \mu s\right) \text{ for one CPU word (32 bits).}$$

The concept of this organization is illustrated in Figure B which shows a 16-bit word being made available in 4-bit words. The 16-bit word is written simultaneously into word locations A, B, C, and D by a common write signal. Any 4-bit word may then be selected from these word locations by separate read-enable strobes.

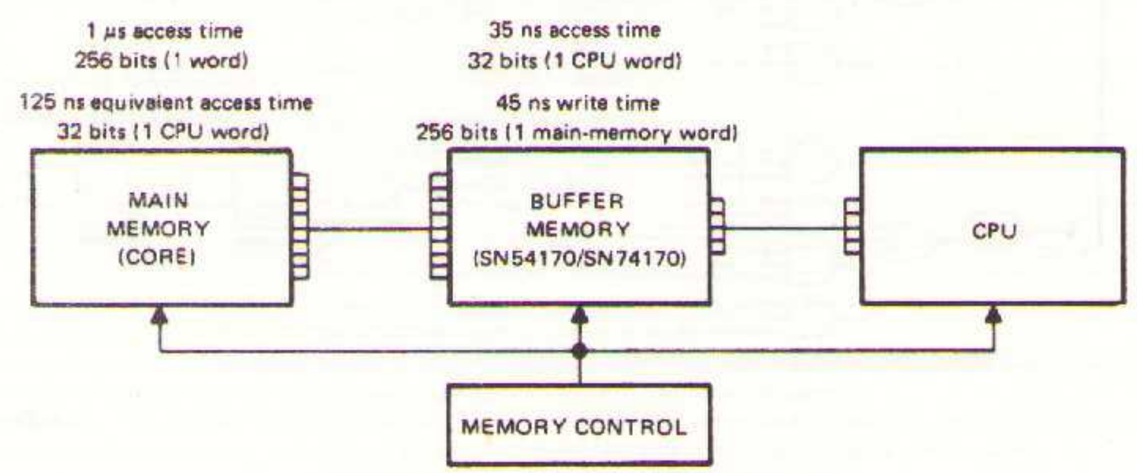


FIGURE A–HIGH-SPEED BUFFER MEMORY

TYPICAL APPLICATION DATA

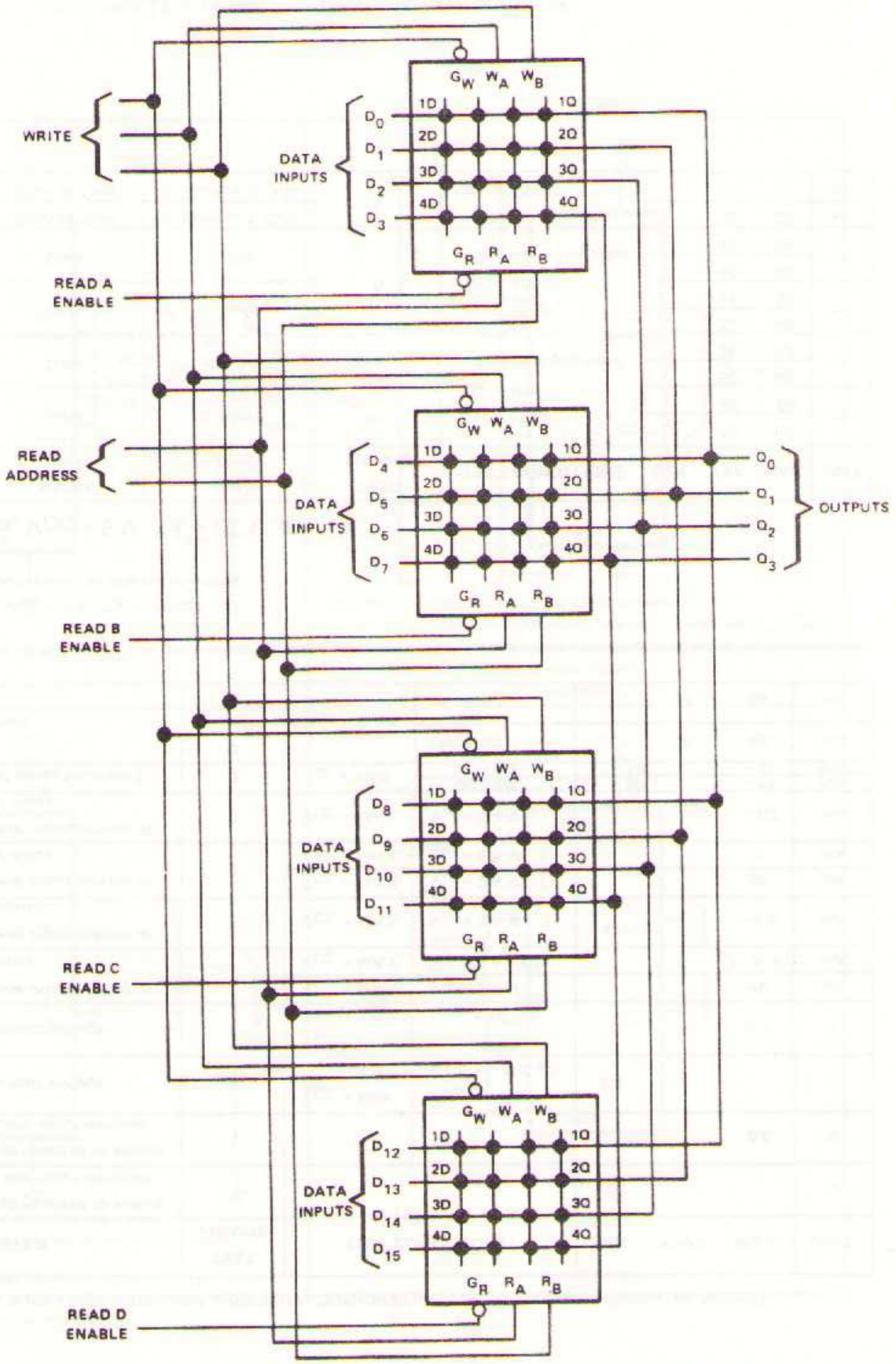


FIGURE B—TYPICAL 16-BIT-WORD-TO-4-BIT-WORD BUFFER MEMORY

logic

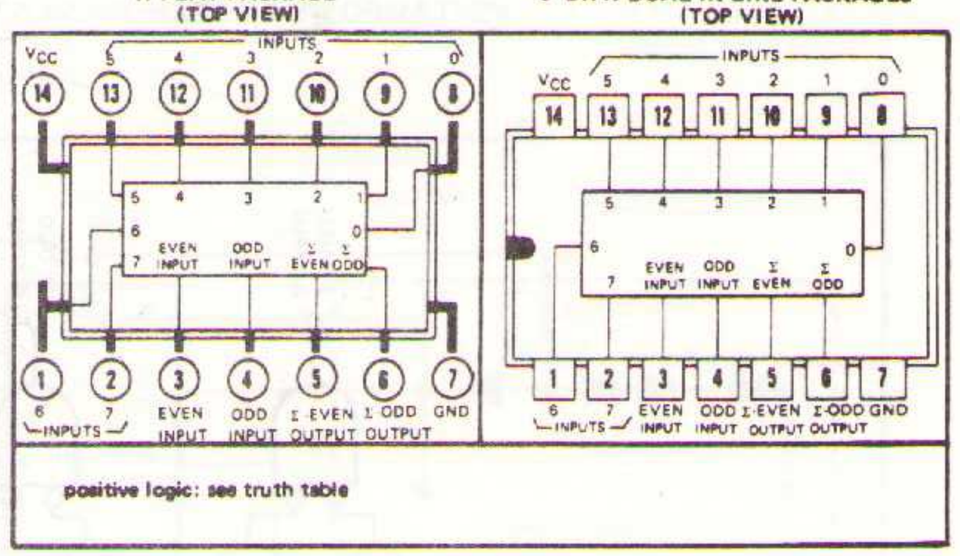
TRUTH TABLE

INPUTS			OUTPUTS	
Σ OF 1's AT 0 THRU 7	EVEN	ODD	Σ EVEN	Σ ODD
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = irrelevant

W FLAT PACKAGE (TOP VIEW)

J OR N DUAL-IN-LINE PACKAGES (TOP VIEW)



description

These universal, monolithic, 8-bit parity generators/checkers, utilizing familiar Series 54/74 TTL circuitry, feature odd/even outputs and control inputs to facilitate operation in either odd- or even-parity applications. The word-length capability is easily expanded by cascading. Typical applications are shown for these parity circuits being used to generate and check parity.

The SN54180/74180 are fully compatible with other TTL or DTL circuits. Input buffers are provided so that each data input represents only one normalized series 54/74 load. A full fan-out to 10 normalized series 54/74 loads is available from each of the outputs in the logical 0 state. A fan-out to 20 normalized loads is provided in the logical 1 state to facilitate the connection of unused inputs to used inputs. Typical power dissipation is 170 mW.

The SN54180 is characterized for operation over the full military temperature range of −55°C to 125°C; and the SN74180 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply Voltage V_{CC} (See Note 1)		7 V
Input Voltage, V_{in} (See Note 1)		5.5 V
Operating Free-Air Temperature Range:	SN54180 Circuits	−55°C to 125°C
	SN74180 Circuits	0°C to 70°C
Storage Temperature Range		−65°C to 150°C

NOTE 1: These voltage values are with respect to network ground terminal.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply Voltage V_{CC} (See Note 1):	SN54180	4.5	5	5.5	V
	SN74180	4.75	5	5.25	V
Normalized Fan-Out from Each Output (N):	Logical 0			10	V
	Logical 1			20	V

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
$V_{in(1)}$	Input voltage required to ensure logical 1 at any input terminal	1			2			V
$V_{in(0)}$	Input voltage required to ensure logical 0 at any input terminal	1					0.8	V
$V_{out(1)}$	Logical 1 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{load} = −800 μA		2.4			V
$V_{out(0)}$	Logical 0 output voltage	1	V_{CC} = MIN, $V_{in(1)}$ = 2 V, $V_{in(0)}$ = 0.8 V, I_{sink} = 16 mA				0.4	V
$I_{in(1)}$	Logical 1 level input current at each data input	2	V_{CC} = MAX, V_{in} = 2.4 V				40	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at each data input	2	V_{CC} = MAX, V_{in} = 0.4 V				−1.6	mA
$I_{in(1)}$	Logical 1 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 2.4 V				80	μA
			V_{CC} = MAX, V_{in} = 5.5 V				1	mA
$I_{in(0)}$	Logical 0 level input current at even or odd input	2	V_{CC} = MAX, V_{in} = 0.4 V				−3.2	mA
I_{OS}	Short circuit output current§	3	V_{CC} = MAX	SN54180	−20		−55	mA
				SN74180	−18		−55	mA
I_{CC}	Supply current	3 and 4	V_{CC} = MAX	SN54180		34	49	mA
				SN74180		34	56	mA

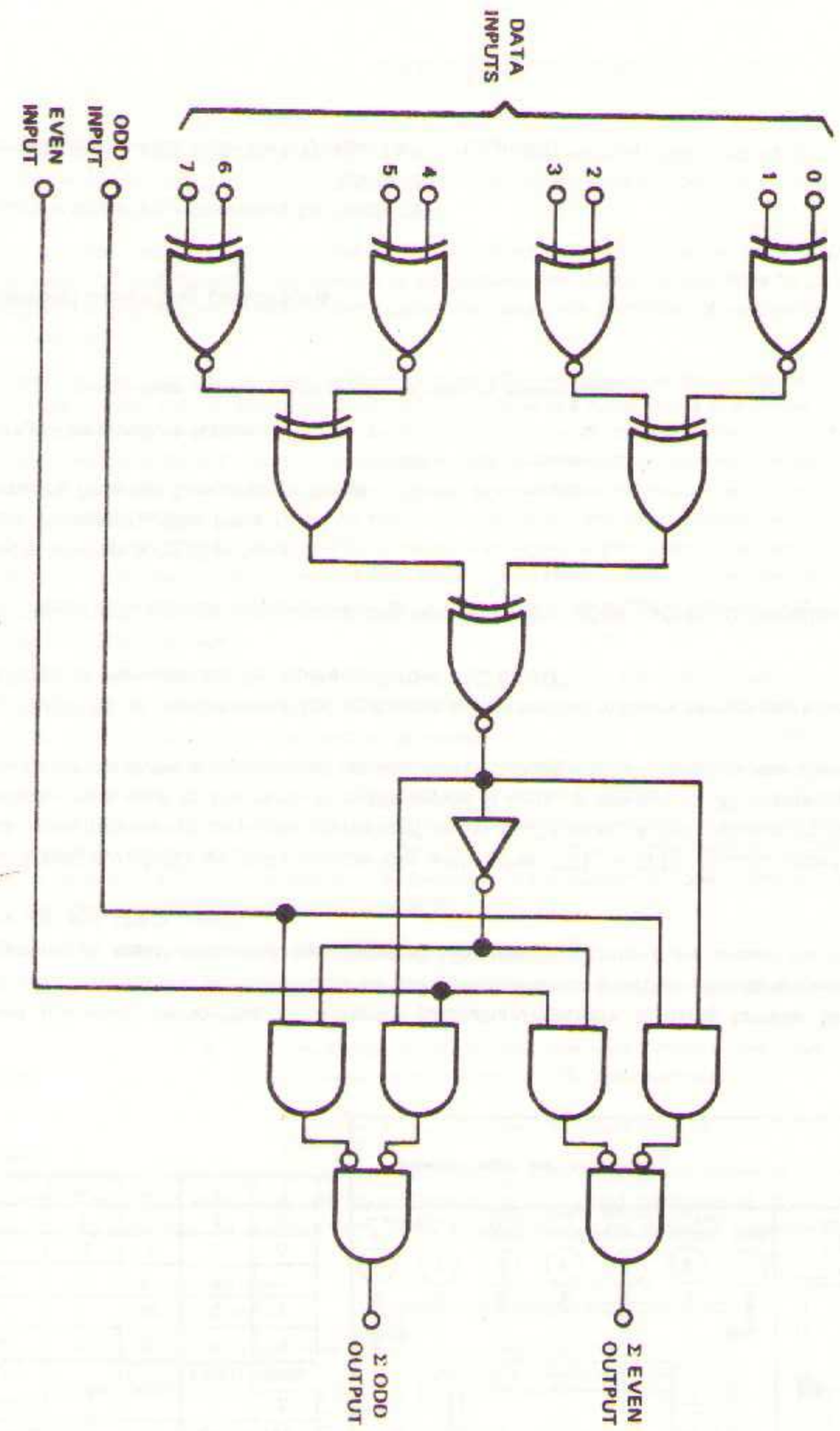
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the particular circuit type.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω, Odd input grounded		40	60	ns
t_{pd0}						45	68	
t_{pd1}	Data	Σ Odd				32	48	ns
t_{pd0}						25	38	
t_{pd1}	Data	Σ Even	5	C_L = 15 pF, R_L = 400 Ω, Even input grounded		32	48	ns
t_{pd0}						25	38	
t_{pd1}	Data	Σ Odd				40	60	ns
t_{pd0}						45	68	
t_{pd1}	Even or Odd	Σ Even or Σ Odd	5	C_L = 15 pF, R_L = 400 Ω		13	20	ns
t_{pd0}	Even or Odd	Σ Even or Σ Odd				7	10	ns



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

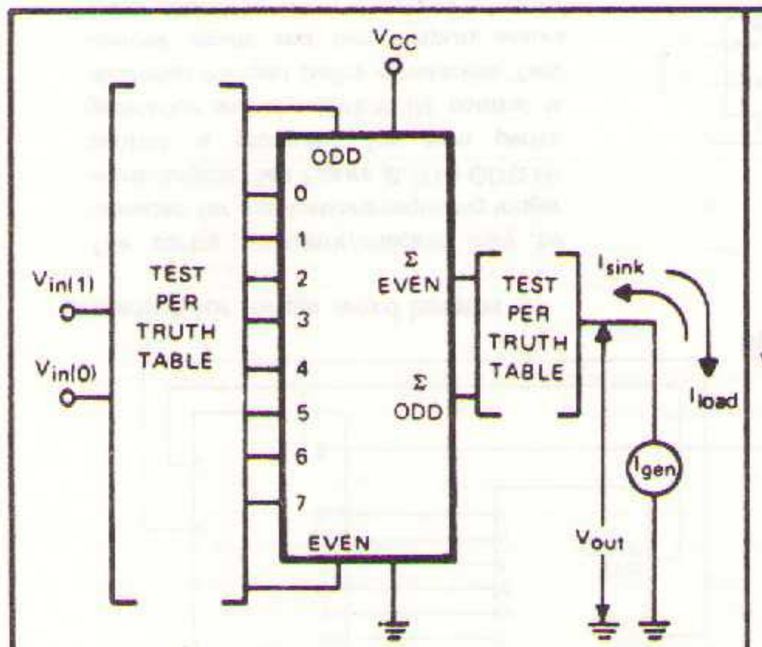
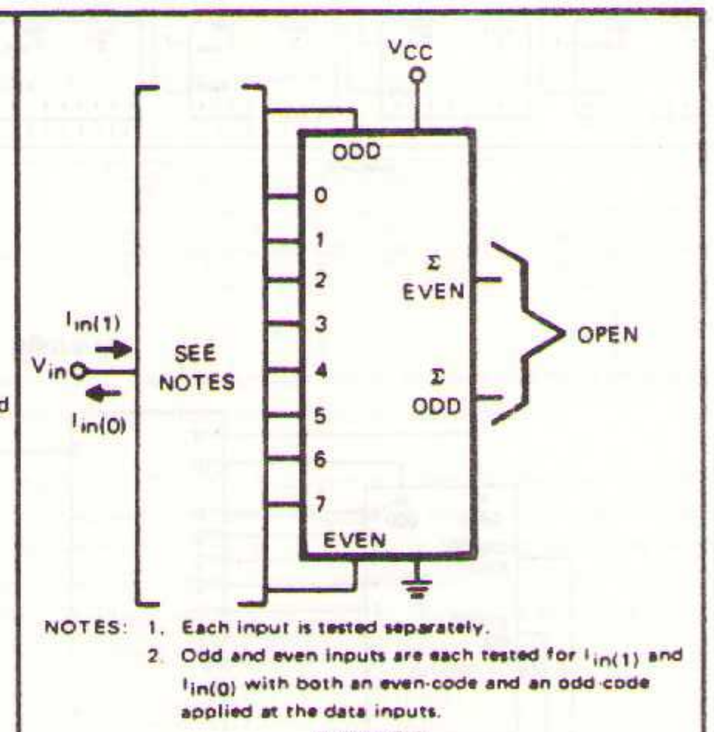
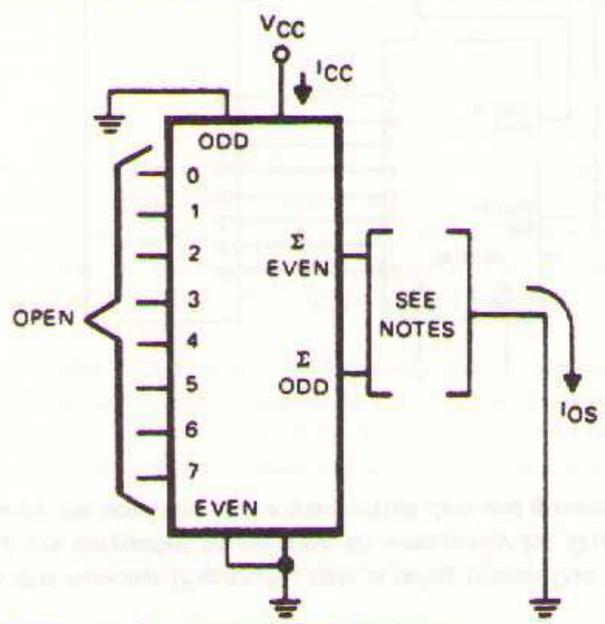


FIGURE 1



NOTES: 1. Each input is tested separately.
2. Odd and even inputs are each tested for $I_{in(1)}$ and $I_{in(0)}$ with both an even-code and an odd-code applied at the data inputs.

FIGURE 2



NOTES: 1. Each output is tested separately.
2. When testing I_{CC} both outputs are open.

FIGURE 3

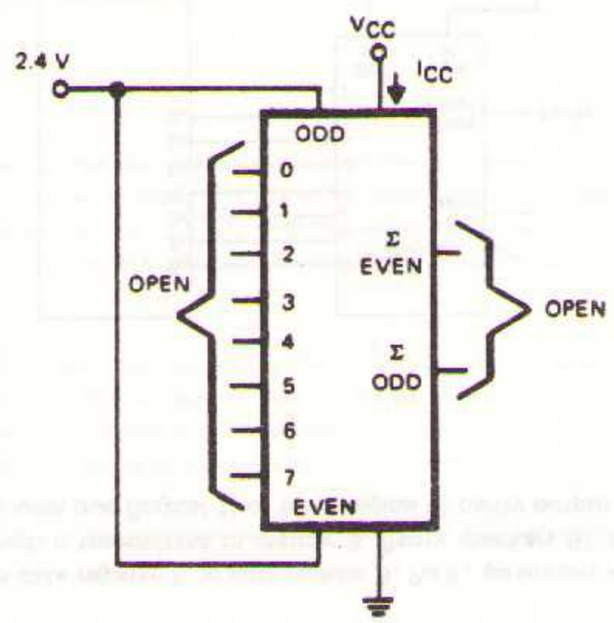
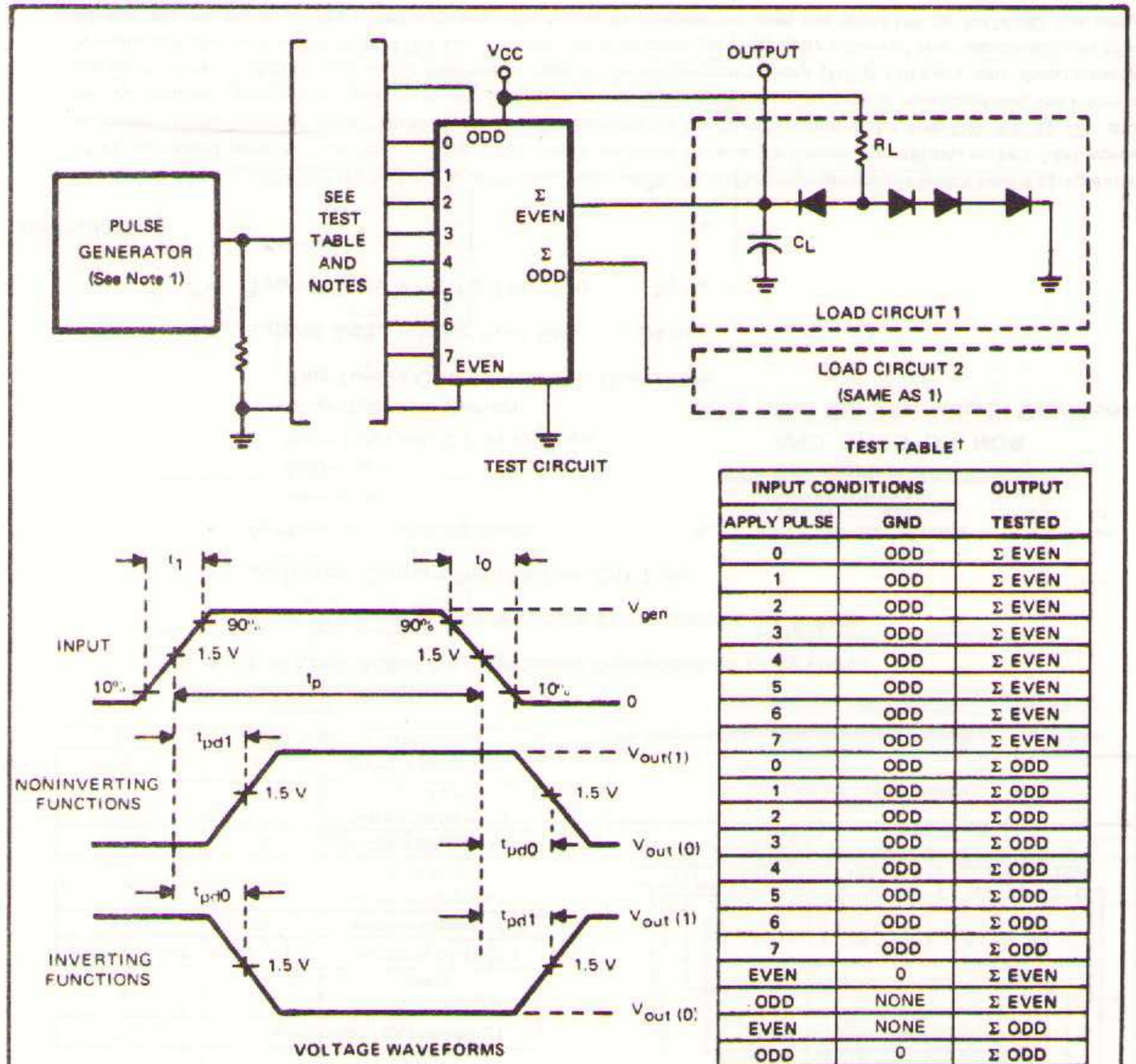


FIGURE 4

†Arrows indicate actual direction of current flow.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST TABLE†

INPUT CONDITIONS		OUTPUT
APPLY PULSE	GND	TESTED
0	ODD	Σ EVEN
1	ODD	Σ EVEN
2	ODD	Σ EVEN
3	ODD	Σ EVEN
4	ODD	Σ EVEN
5	ODD	Σ EVEN
6	ODD	Σ EVEN
7	ODD	Σ EVEN
0	ODD	Σ ODD
1	ODD	Σ ODD
2	ODD	Σ ODD
3	ODD	Σ ODD
4	ODD	Σ ODD
5	ODD	Σ ODD
6	ODD	Σ ODD
7	ODD	Σ ODD
EVEN	0	Σ EVEN
ODD	NONE	Σ EVEN
EVEN	NONE	Σ ODD
ODD	0	Σ ODD

†Repeat all but the last 4 tests with the even input grounded.

NOTES: 1. The pulse generator has the following characteristics: V_{gen} = 3 V, $t_r = t_f$ = 10 ns, t_p = 500 ns, PRR = 1 MHz, and $Z_{out} \approx 50\ \Omega$.
2. Inputs not specified are open.
3. C_L includes probe and jig capacitance.
4. All diodes are 1N3064.

FIGURE 5 – SWITCHING TIMES

TYPICAL APPLICATIONS

verifying transmitted data

In this example (Figure A), data is being transmitted from data register A to data register B. Parity generators A1 and A2 are connected to generate an even-parity bit Q_{16} which is transmitted to register B. Parity checkers B1 and B2 verify the accuracy of the transmitted data and generate an even true (logical 1) or false (logical 0) parity output signal.

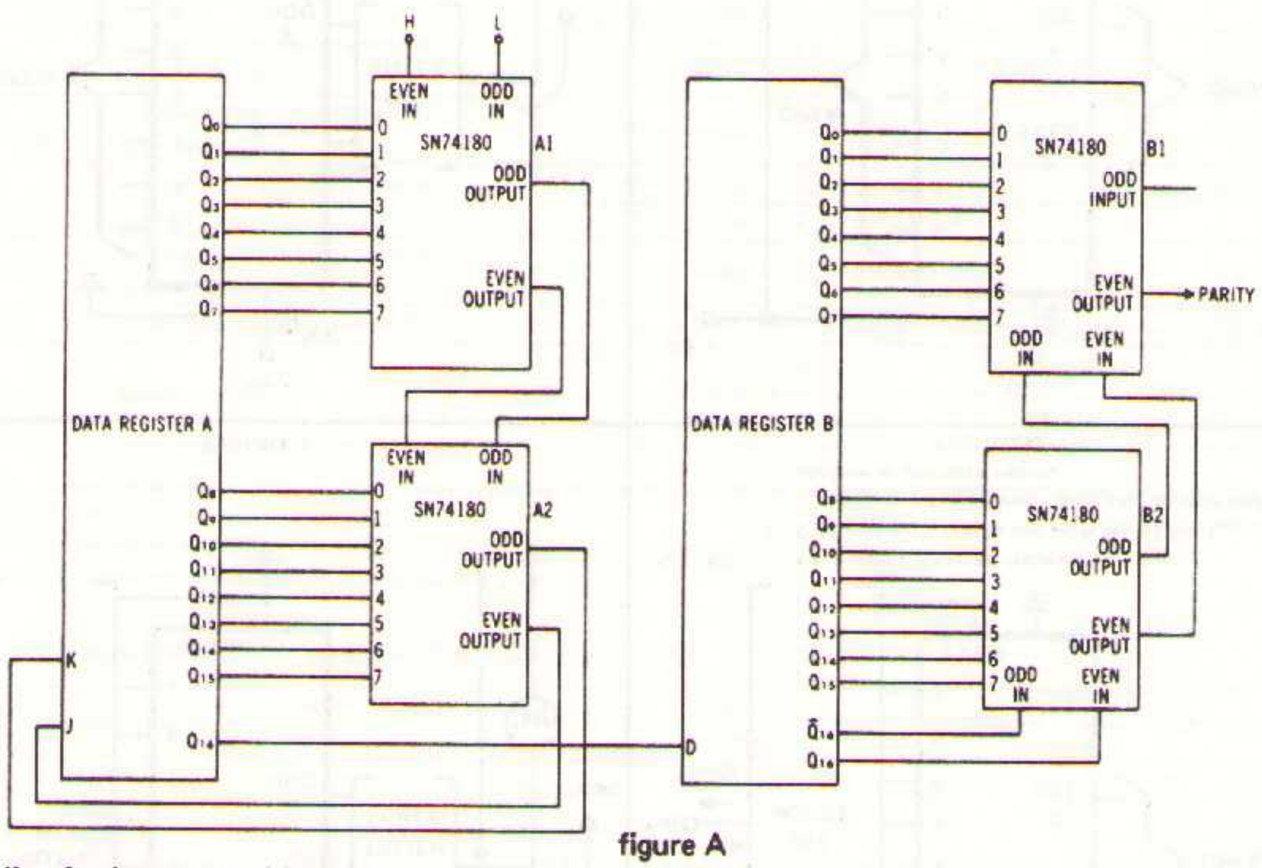


figure A

cascading for longer word lengths

The parity generator/checker may be cascaded for applications requiring longer word lengths. See Figure B. The ODD IN control is grounded for even parity generation and the EVEN IN control is grounded for odd parity generation. Two control inputs and two outputs ensure faster operation when cascading for word lengths over 8 bits, as only one gate delay is added for each additional 8-bit group. For a 32-bit word, parity can be generated in approximately 65 ns.

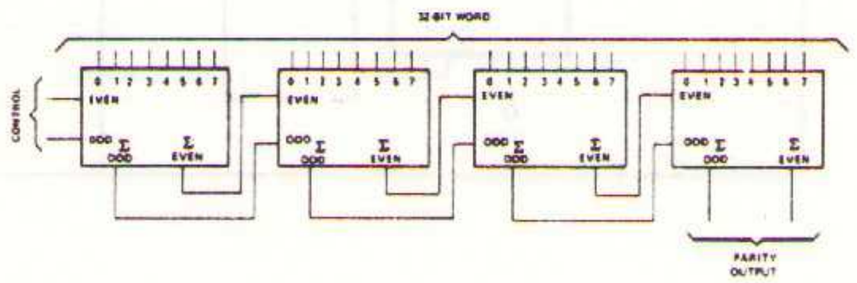
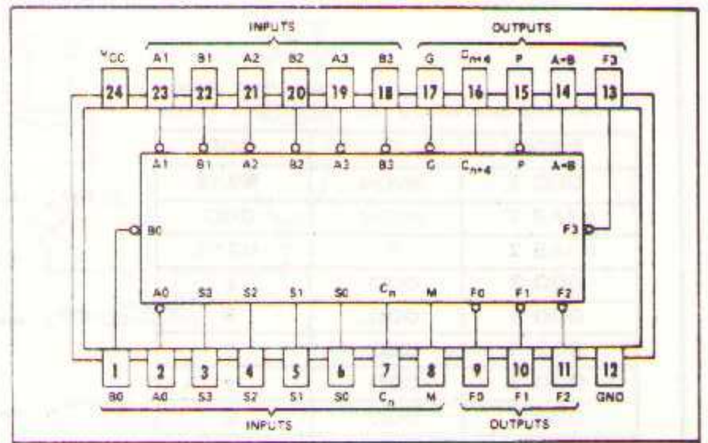


figure B

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
A3, A2, A1, A0	19, 21, 23, 2	WORD A INPUTS
B3, B2, B1, B0	18, 20, 22, 1	WORD B INPUTS
S3, S2, S1, S0	3, 4, 5, 6	FUNCTION-SELECT INPUTS
C_n	7	INV. CARRY INPUT
M	8	MODE CONTROL INPUT
F3, F2, F1, F0	13, 11, 10, 9	FUNCTION OUTPUTS
A = B	14	COMPARATOR OUTPUT
P	15	CARRY PROPAGATE OUTPUT
C_{n+4}	16	INV. CARRY OUTPUT
G	17	CARRY GENERATE OUTPUT
V_{CC}	24	SUPPLY VOLTAGE
GND	12	GROUND

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



logic: see function tables

†Pin assignments for these circuits are the same for all packages.

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects
- Darlington Outputs Reduce Turn-Off Time
- Arithmetic Operating Modes:
  - Addition
  - Subtraction
  - Shift Operand A One Position
  - Magnitude Comparison
  - Plus Twelve Other Arithmetic Operations
- Logic Function Modes:
  - Exclusive-OR
  - Comparator
  - AND, NAND, OR, NOR
  - Plus Ten Other Logical Operations
- Typical Add Time for Four Bits . . . . 24 ns
- Typical Carry Time for Four Bits . . . . 12 ns

description

The SN54181 and SN74181 are high-speed arithmetic logic units (ALU)/function generators which have a complexity of 75 equivalent gates on a monolithic chip. This circuit performs 16 binary arithmetic operations on two 4-bit words as shown in the function table. These operations are selected by the four function-select lines (S0, S1, S2, S3) and include addition, subtraction, decrement, and straight transfer. When performing arithmetic manipulations, the internal carries must be enabled by applying a low-level voltage to the mode control input (M). A full carry look-ahead scheme is made available in the SN54/SN74181 for fast, simultaneous carry generation by means of two cascade-outputs (pin 15 and 17) for the four bits in the package. When used in conjunction with the SN54182 or SN74182 full carry look-ahead circuits, high-speed arithmetic operations can be performed. For example, the typical addition time for the SN54181/SN74181 is 24 nanoseconds for four bits. When expanding to 16-bit addition with the SN54182/SN74182, only 13 nanoseconds further delay is added so that the total addition time is 37 nanoseconds, or 2.2 nanoseconds per bit. One SN54182/SN74182 is needed for every 16 bit (four SN54181/SN74181 circuits).

If high speed is not of importance, a ripple-carry input (C_n) and a ripple-carry output (C_{n+4}) are available. However, the ripple-carry delay has also been minimized so that arithmetic manipulations for small word lengths can be

performed without external circuitry. The typical delay for the ripple carry is 12 nanoseconds for four bits. With a typical addition time of 24 nanoseconds for four bits, addition of two 8-bit words is accomplished typically in 36 nanoseconds when employing the ripple carry.

The SN54181 and SN74181 will accommodate active-high or active-low data if the pin-designations are reinterpreted as follows:

PIN NUMBER	2	1	23	22	21	20	19	18	9	10	11	13	7	16	15	17
Active-high data (Figure I)	A_0	B_0	A_1	B_1	A_2	B_2	A_3	B_3	F_0	F_1	F_2	F_3	$\overline{C_n}$	$\overline{C_{n+4}}$	X	Y
Active-low data (Figure II)	$\overline{A_0}$	$\overline{B_0}$	$\overline{A_1}$	$\overline{B_1}$	$\overline{A_2}$	$\overline{B_2}$	$\overline{A_3}$	$\overline{B_3}$	$\overline{F_0}$	$\overline{F_1}$	$\overline{F_2}$	$\overline{F_3}$	C_n	C_{n+4}	$\overline{P}$	$\overline{G}$

Subtraction is accomplished by 1's complement addition where the 1's complement of the subtrahend is generated internally. The resultant output is A−B−1 which requires an end-around or forced carry to provide A−B.

The SN54181 or SN74181 can also be utilized as a comparator. The A = B output is internally decoded from the function outputs (F0, F1, F2, F3) so that when two words of equal magnitude are applied at the A and B inputs, it will assume a high-level state to indicate equality (A = B). The SN54181/SN74181 should be in the subtract mode when performing this comparison. The A = B output is open-collector so that it can be wire-AND connected to give a comparison for more than four bits. The carry output (C_{n+4}) can also be used to supply relative magnitude information. Again, the ALU should be placed in the subtract mode by placing the control lines at LHHL.

	Input C_n	Output C_{n+4}	Indicates
Active-High Data (Figure I)	H	H	A = B
	L	H	A < B
	H	L	A > B
	L	L	A > B
Active-Low Data (Figure II)	L	L	A > B
	H	L	A < B
	L	H	A > B
	H	H	A = B

These circuits have been designed to not only incorporate all of the designer's requirements for arithmetic operations, but also to provide 16 possible functions of two Boolean variables without the use of external circuitry. These logic functions are selected by use of the four function-select inputs (S0, S1, S2, S3) with the mode control input (M) at a high level to disable the internal carry. The 16 logic functions are detailed in the function table and include exclusive-OR, NAND, AND, NOR, and OR functions.

The SN54181/SN74181 is designed with a Darlington output configuration (54H/74H type) to reduce the high-logic-level output impedance and thereby improve the turn-off propagation delay time. All outputs are rated at a normalized fan-out of ten at the low logic level and increased to a fan-out of 20 at the high logic level. The increased high-logic-level fan-out allows the system designer more freedom in tying unused inputs to driven inputs.

The SN54181 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74181 is characterized for operation from 0°C to 70°C.

ALU Signal Designations

The SN54181 and SN74181 can be used with either the signal designations as shown in Figures I or II.

The logic functions and arithmetic operations obtained with signal designations as in Figure I are given in Table I; those obtained with the signal designations of Figure II are given in Table II.

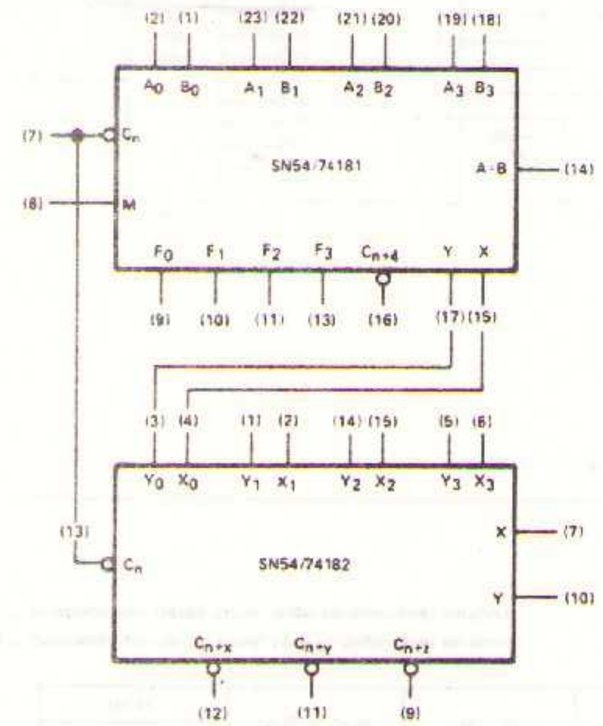


FIGURE I
(FOR TABLE I)

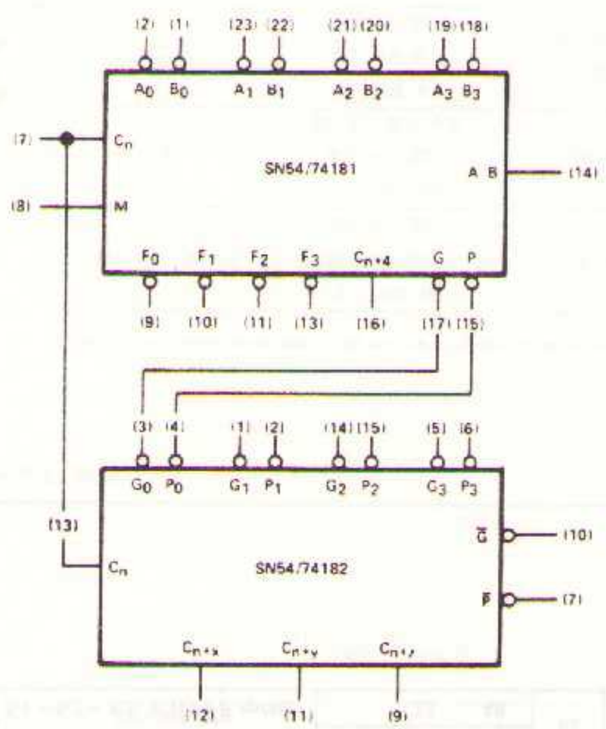


FIGURE II
(FOR TABLE II)

TABLE I

SELECTION S_3 S_2 S_1 S_0	ACTIVE-HIGH DATA: M = H LOGIC FUNCTIONS	M = L: ARITHMETIC OPERATIONS: $C_n = 0$, $\overline{C_n} = 1 = H$	$C_n = 1$, $\overline{C_n} = 0 = L$
L L L L	$F = \overline{A}$	F = A	F = A PLUS 1
L L L H	$F = \overline{A + B}$	F = A + B	F = (A + B) PLUS 1
L L H L	$F = \overline{A}B$	$F = A + \overline{B}$	F = (A + $\overline{B}$) PLUS 1
L L H H	F = 0	F = MINUS 1 (2's COMPL)	F = ZERO
L H L L	$F = \overline{AB}$	$F = A \text{ PLUS } A\overline{B}$	$F = A \text{ PLUS } A\overline{B} \text{ PLUS } 1$
L H L H	$F = \overline{B}$	$F = (A + B) \text{ PLUS } A\overline{B}$	$F = (A + B) \text{ PLUS } A\overline{B} \text{ PLUS } 1$
L H H L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = A\overline{B}$	$F = A\overline{B} \text{ MINUS } 1$	$F = A\overline{B}$
H L L L	$F = \overline{A} + B$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = (A + $\overline{B}$) PLUS AB	F = (A + $\overline{B}$) PLUS AB PLUS 1
H L H H	F = AB	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	$F = A + \overline{B}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	F = A + B	F = (A + $\overline{B}$) PLUS A	F = (A + $\overline{B}$) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

TABLE II

SELECTION S_3 S_2 S_1 S_0	ACTIVE LOW DATA: M = H LOGIC FUNCTIONS	M = L: ARITHMETIC OPERATIONS: $C_n = 0$, $C_n = 0 = L$	$C_n = 1$, $C_n = 1 = H$
L L L L	F = $\overline{A}$	F = A MINUS 1	F = A
L L L H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L L H L	F = $\overline{A} + B$	F = AB MINUS 1	F = AB
L L H H	F = 1	F = MINUS 1 (2's COMP)	F = ZERO
L H L L	$F = \overline{A + B}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
L H L H	F = $\overline{B}$	F = AB PLUS (A + $\overline{B}$)	F = AB PLUS (A + $\overline{B}$) PLUS 1
L H H L	$F = \overline{A \oplus B}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	F = A + $\overline{B}$	F = A + $\overline{B}$	F = (A + $\overline{B}$) PLUS 1
H L L L	F = $\overline{A}B$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	$F = \overline{A \oplus B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	F = B	F = $A\overline{B}$ PLUS (A + B)	F = $A\overline{B}$ PLUS (A + B) PLUS 1
H L H H	F = A + B	F = A + B	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A*	F = A PLUS A PLUS 1
H H L H	F = $A\overline{B}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	F = AB	F = $A\overline{B}$ PLUS A	F = $A\overline{B}$ PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

* Each bit is shifted to the next more significant position.

absolute maximum ratings over operating temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range:	SN54181 Circuits	−55°C to 125°C
	SN74181 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple emitter transistor. For this circuit, this rating applies to each A input in conjunction with inputs S2 or S3, and to each B input in conjunction with inputs S0 or S3.

recommended operating conditions

		SN54181			SN74181			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage any output except A = B	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
I_{OH}	High-level output current, A = B output only	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, V_{OH} = 5.5 V				250	μA
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_{IH}	High-level input current (mode input)	3	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IH}	High-level input current (any A or B input)	3	V_{CC} = MAX, V_I = 2.4 V				120	μA
I_{IH}	High-level input current (any S input)	3	V_{CC} = MAX, V_I = 2.4 V				160	μA
I_{IH}	High-level input current (carry input)	3	V_{CC} = MAX, V_I = 2.4 V				200	μA
I_{IH}	High-level input current (any input)	3	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IL}	Low-level input current (mode input)	3	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{IL}	Low-level input current (any A or B input)	3	V_{CC} = MAX, V_I = 0.4 V				−4.8	mA
I_{IL}	Low-level input current (any S input)	3	V_{CC} = MAX, V_I = 0.4 V				−6.4	mA
I_{IL}	Low-level input current (carry input)	3	V_{CC} = MAX, V_I = 0.4 V				−8	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX	SN54181	−20		−55	mA
				SN74181	−18		−57	
I_{CC}	Supply current	5	V_{CC} = MAX	SN54181		88	127	mA
				SN74181		88	140	
I_{CC}	Supply current	6	V_{CC} = MAX	SN54181		94	135	mA
				SN74181		94	150	

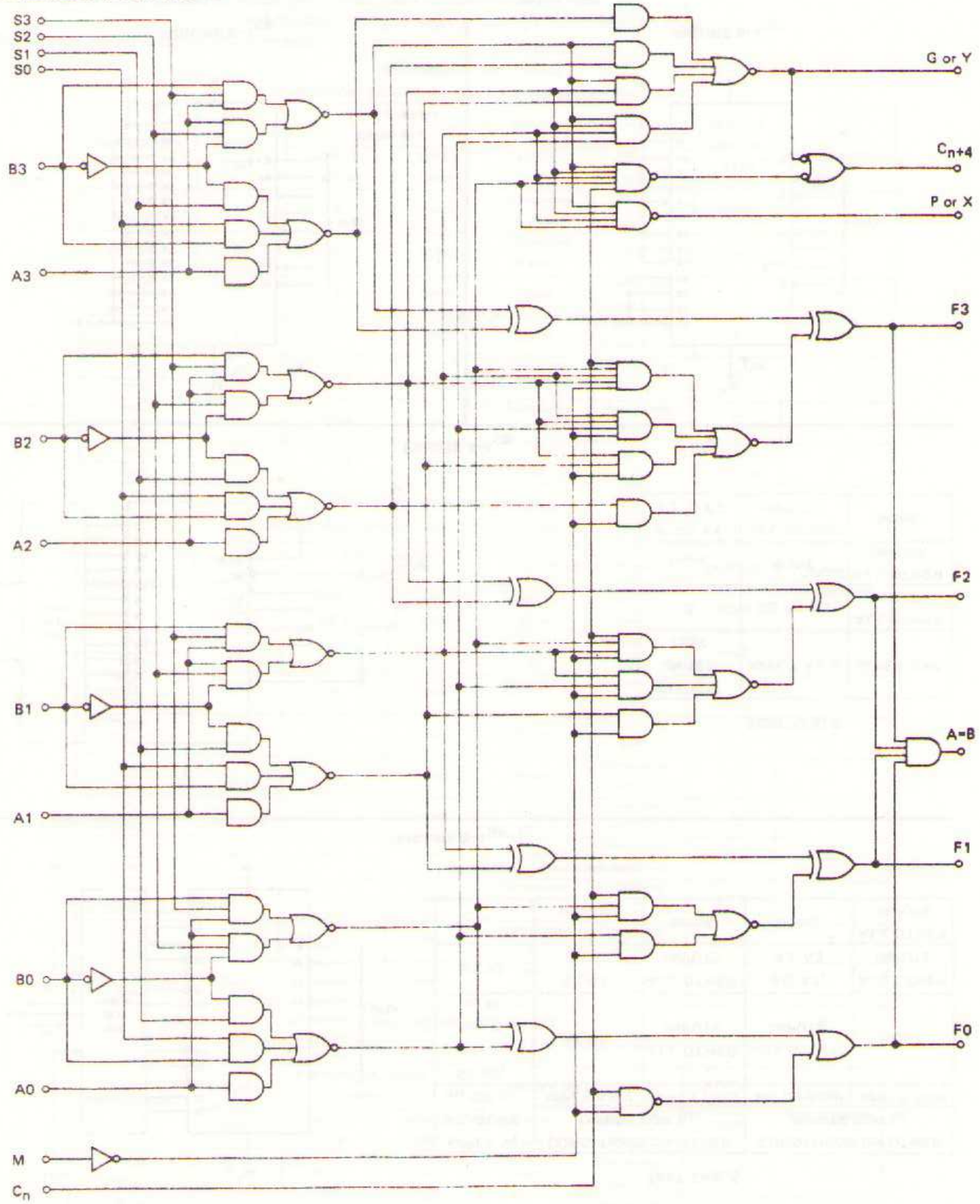
† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10 (C_L = 15 pF, R_L = 400 Ω)

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	C_n	C_{n+4}	7			12	18	ns
t_{PHL}						13	19	
t_{PLH}	C_n	Any F	7	M = 0 V ($\overline{SUM}$ or $\overline{DIFF}$ mode)		13	19	ns
t_{PHL}						12	18	
t_{PLH}	Any A or B	G	7	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}						13	19	
t_{PLH}	Any A or B	G	7	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	P	7	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		13	19	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	P	7	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		17	25	ns
t_{PHL}						17	25	
t_{PLH}	Any A or B	Any F	7	M = 0 V, S0 = S3 = 4.5 V, S1 = S2 = 0 V ($\overline{SUM}$ mode)		28	42	ns
t_{PHL}						21	32	
t_{PLH}	Any A or B	Any F	7	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		32	48	ns
t_{PHL}						23	34	
t_{PLH}	Any A or B	Any F	7	M = 4.5 V (logic mode)		32	48	ns
t_{PHL}						23	34	
t_{PLH}	Any A or B	A = B	7	M = 0 V, S0 = S3 = 0 V, S1 = S2 = 4.5 V ($\overline{DIFF}$ mode)		35	50	ns
t_{PHL}						32	48	

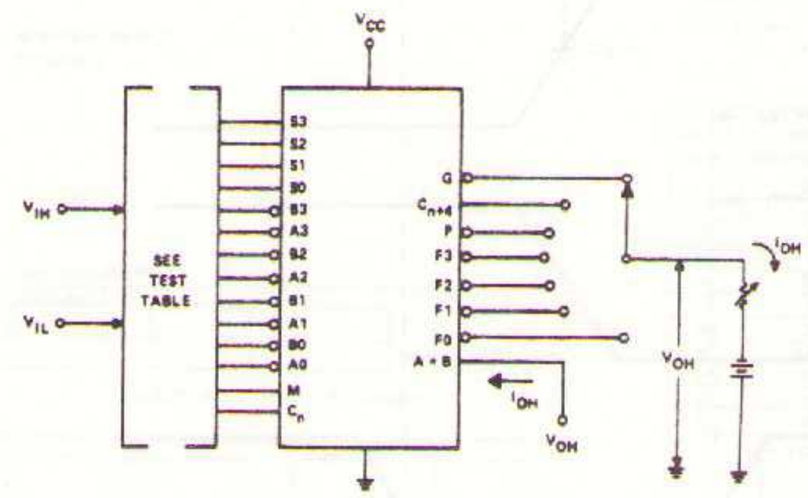
¶ t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

functional block diagram



PARAMETER MEASUREMENT INFORMATION

d-c test circuits†

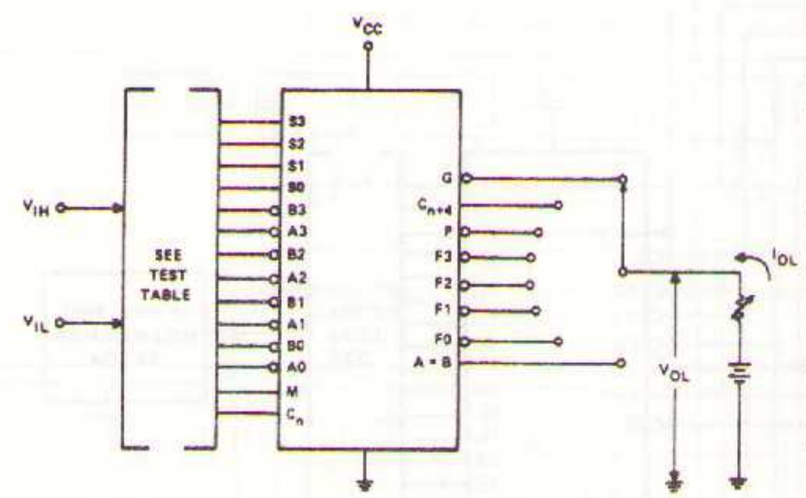


TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
G	S3, B3, A3	S2, S1, S0, B2, A2, B1, A1, B0, A0
C_{n+4}	S3, S2, B3, B2, A2, B1, A1, B0, A0	S1, S0, A3, C_n
P	S3, S2, B3, A3, B2, A2, B1, A1, B0, A0	NONE
any F or A = B	S3, S2, S1, S0, A3, A2, A1, A0, M	NONE

Inputs not otherwise specified are connected to ground.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
G	S3, S2, S0, B2, A2, B1, A1, B0, A0	S1, B3, A3
C_{n+4}	S3, A3, A2, A1, B0, A0	S2, S1, S0, B3, B2, B1
P	S2, B3, A3, B2, A2, B1, A1, B0, A0	S3
any F	S3, S2, S1, S0, M, C_n	A3, A2, A1, A0
A = B	S3, S2, S1, S0, A3, A2, A1, M, C_n	A0

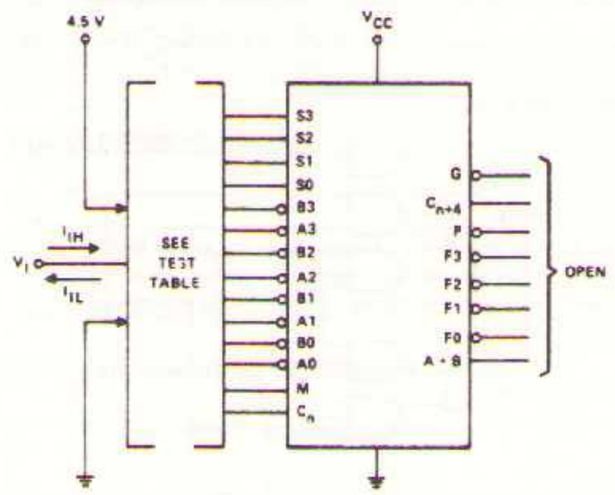
Inputs not otherwise specified are connected to ground.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits† (continued)

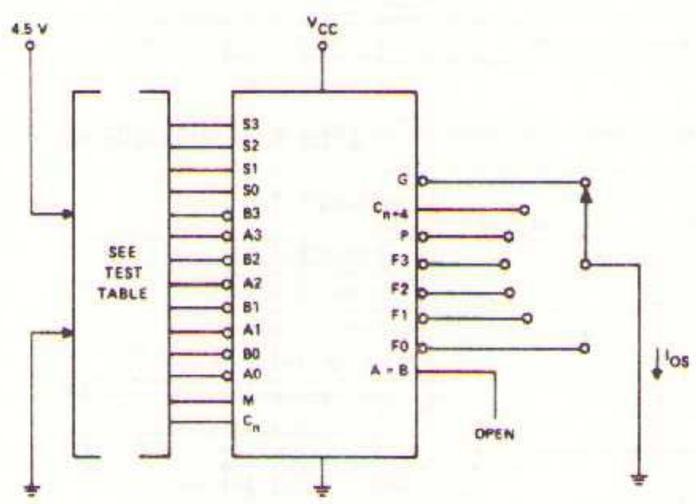


TEST TABLE

APPLY V_I MEASURE	CONDITIONS ON OTHER INPUTS FOR I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
I_{IH} OR I_{IL}	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
S0, S3, any A, any B, or M	NONE	ALL OTHER INPUTS	ALL OTHER INPUTS	NONE
S1, S2	B0, B1, B2, B3	ALL OTHER INPUTS	A0, A1, A2, A3	ALL OTHER INPUTS
C_n	ALL OTHER INPUTS	NONE	NONE	ALL OTHER INPUTS

Each input is tested separately.

FIGURE 3–I_{IH}, I_{IL}



TEST TABLE

OUTPUT UNDER TEST	APPLY 4.5 V	APPLY GND
G	S3, A3, B3	ALL OTHER INPUTS
C_{n+4}	NONE	ALL OTHER INPUTS
P, F0, F1, F2, or F3	ALL OTHER INPUTS	NONE

FIGURE 4–I_{OS}

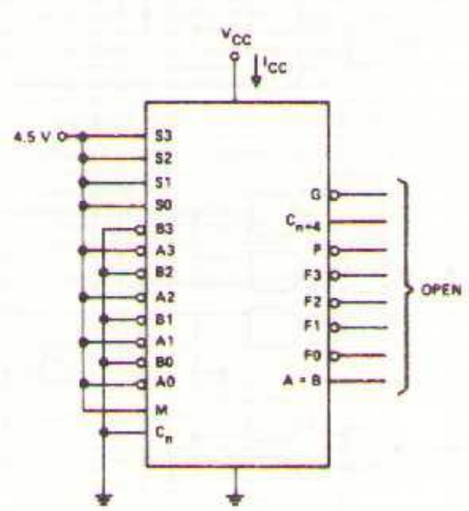


FIGURE 5–I_{CC}

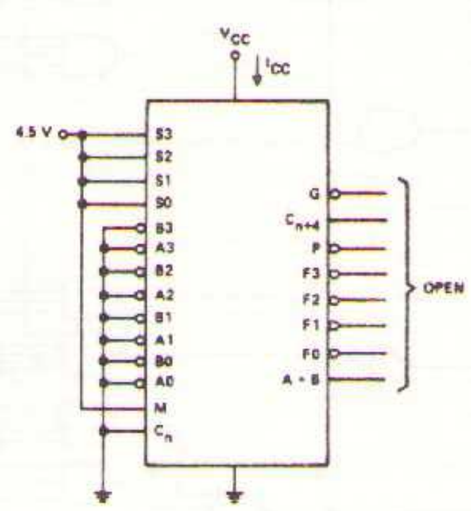
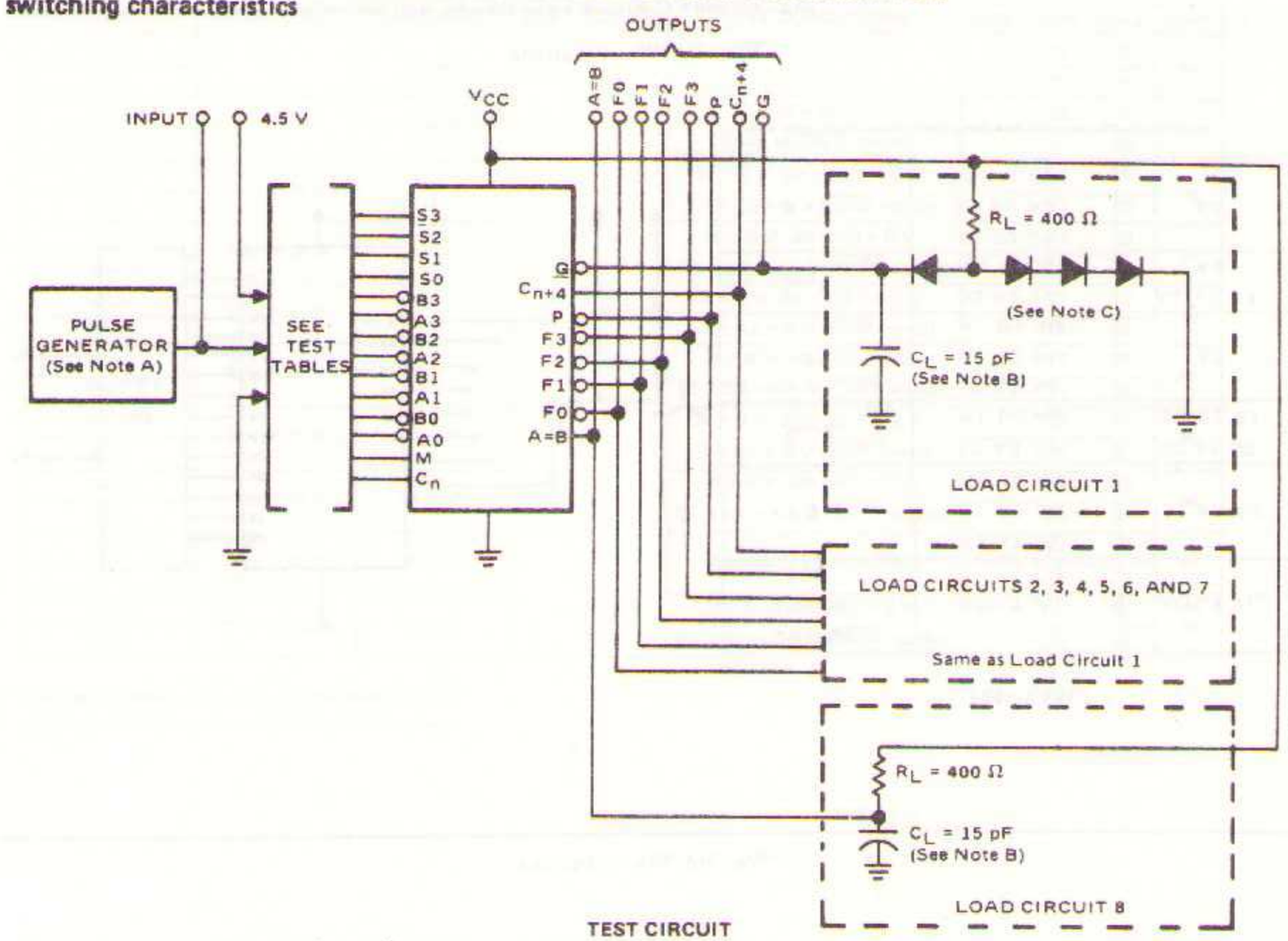


FIGURE 6–I_{CC}

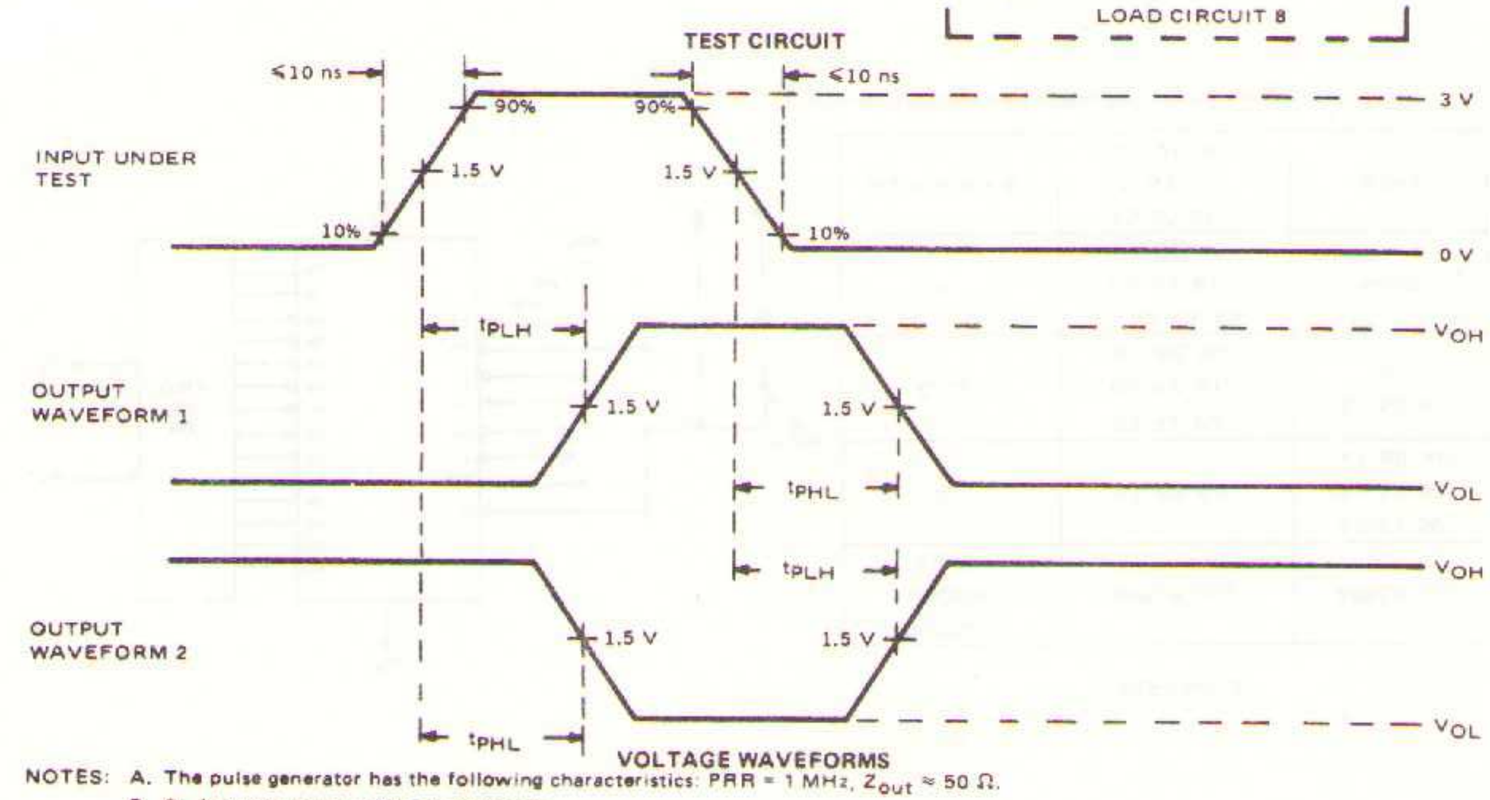
†Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

FIGURE 7–PROPAGATION DELAY TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics (continued)

$\overline{\text{SUM}}$ MODE TEST TABLE

FUNCTION INPUTS: S0 = S3 = 4.5 V, S1 = S2 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	A	B	None	Remaining A and B	C_n	Any F	1
t_{PLH} t_{PHL}	B	A	None	Remaining A and B	C_n	Any F	1
t_{PLH} t_{PHL}	A	B	None	None	Remaining A and B, C_n	P	1
t_{PLH} t_{PHL}	B	A	None	None	Remaining A and B, C_n	P	1
t_{PLH} t_{PHL}	A	None	B	Remaining B	Remaining A, C_n	G	1
t_{PLH} t_{PHL}	B	None	A	Remaining B	Remaining A, C_n	G	1
t_{PLH} t_{PHL}	C_n	None	None	All A	All B	Any F or C_{n+4}	1

$\overline{\text{DIFF}}$ MODE TEST TABLE

FUNCTION INPUTS: S1 = S2 = 4.5 V, S0 = S3 = M = 0 V

PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	A	None	B	Remaining A	Remaining B, C_n	Any F	1
t_{PLH} t_{PHL}	B	A	None	Remaining A	Remaining B, C_n	Any F	2
t_{PLH} t_{PHL}	A	None	B	None	Remaining A and B, C_n	P	1
t_{PLH} t_{PHL}	B	A	None	None	Remaining A and B, C_n	P	2
t_{PLH} t_{PHL}	A	B	None	None	Remaining A and B, C_n	G	1
t_{PLH} t_{PHL}	B	None	A	None	Remaining A and B, C_n	G	2
t_{PLH} t_{PHL}	A	B	None	Remaining A	Remaining B, C_n	A = B	2
t_{PLH} t_{PHL}	B	A	None	Remaining A	Remaining B, C_n	A = B	2
t_{PLH} t_{PHL}	C_n	None	None	All A and B	None	C_{n+4}	2

LOGIC MODE TEST TABLE

FUNCTION INPUTS: S1 = S3 = M = 4.5 V, S0 = S2 = 0 V

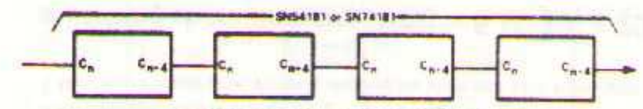
PARAMETER	INPUT UNDER TEST	OTHER INPUT SAME BIT		OTHER DATA INPUTS		OUTPUT UNDER TEST	OUTPUT WAVEFORM
		APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND		
t_{PLH} t_{PHL}	A	None	B	None	Remaining A and B, C_n	Any F	2
t_{PLH} t_{PHL}	B	None	A	None	Remaining A and B, C_n	Any F	2

TYPICAL APPLICATION DATA

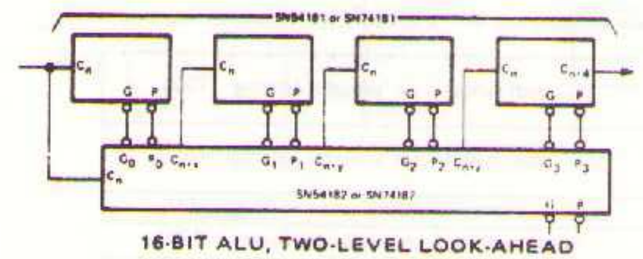
Typical addition times for various configurations are given in the table below. Subtraction times are in the same range as summation times.

TYPICAL ADDITION TIMES

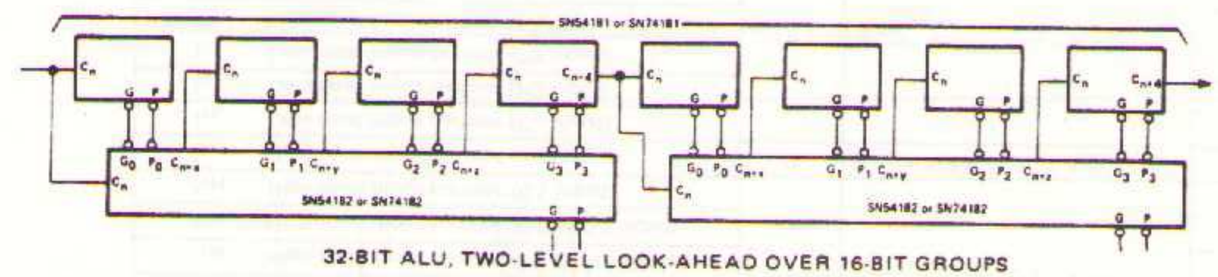
NO. OF BITS	TOTAL ADDITION TIME (ns)	ADD TIME PER BIT (ns)	PACKAGE COUNT SN54181/ SN74181	PACKAGE COUNT SN54182/ SN74182	CARRY BETWEEN ALU's
4	24	6.0	1		NONE
8	36	4.5	2		RIPPLE
12	48	4.0	3		RIPPLE
12	36	3.0	3	1	FULL LOOK-AHEAD
16	60	3.8	4		RIPPLE
16	36	2.2	4	1	FULL LOOK-AHEAD
32	120	3.8	8		RIPPLE
32	96	3.0	8	1	PARTIAL LOOK-AHEAD
32	72	2.2	8	2	PARTIAL LOOK-AHEAD
32	60	1.9	8	3	FULL LOOK-AHEAD



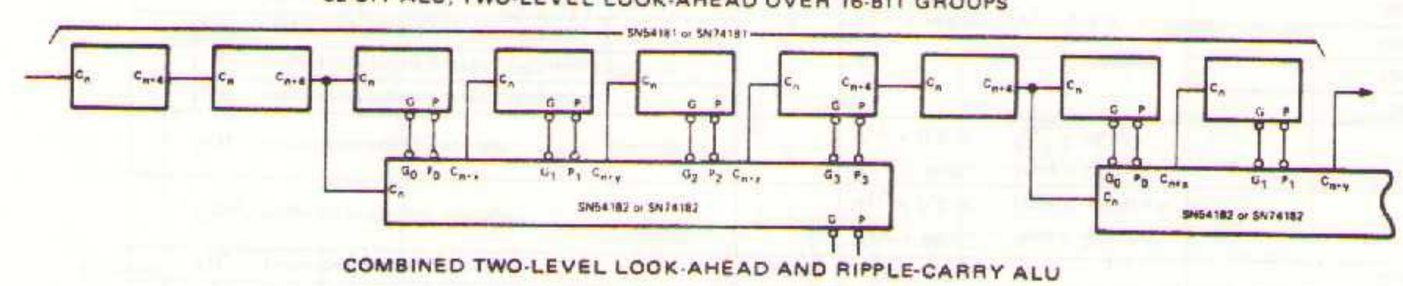
16-BIT ALU, RIPPLE CARRY



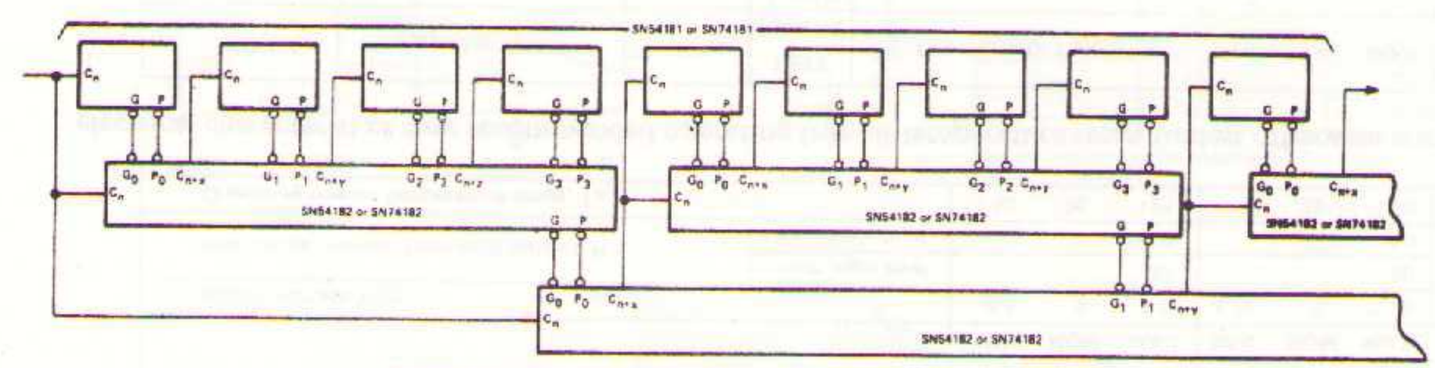
16-BIT ALU, TWO-LEVEL LOOK-AHEAD



32-BIT ALU, TWO-LEVEL LOOK-AHEAD OVER 16-BIT GROUPS



COMBINED TWO-LEVEL LOOK-AHEAD AND RIPPLE-CARRY ALU



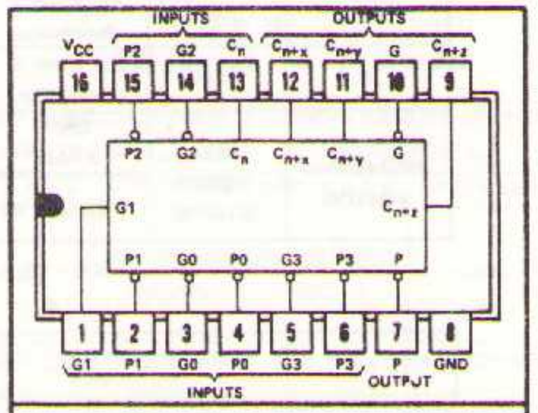
64-BIT ALU, FULL-CARRY LOOK-AHEAD IN THREE LEVELS

A and B inputs and F outputs are not shown.

PIN DESIGNATIONS

DESIGNATION	PIN NOS.	FUNCTION
G0, G1, G2, G3	3, 1, 14, 5	ACTIVE-LOW CARRY GENERATE INPUTS
P0, P1, P2, P3	4, 2, 15, 6	ACTIVE-LOW CARRY PROPAGATE INPUTS
C_n	13	CARRY INPUT
C_{n+x}, C_{n+y}, C_{n+z}	12, 11, 9	CARRY OUTPUTS
G	10	ACTIVE-LOW CARRY GENERATE OUTPUT
P	7	ACTIVE-LOW CARRY PROPAGATE OUTPUT
V_{CC}	16	SUPPLY VOLTAGE
GND	8	GROUND

J OR N DUAL-IN-LINE OR W FLAT PACKAGE (TOP VIEW)†



logic: see description

†Pin assignments for these circuits are the same for all packages.

description

The SN54182, SN74182 is a high-speed, look-ahead carry generator capable of anticipating a carry across four binary adders or group of adders. It is cascadable to perform full look-ahead across n-bit adders, with only 13 nanoseconds delay for each level of look-ahead. Carry, generate-carry, and propagate-carry functions are provided as enumerated in the pin designation table above.

The SN54182 or SN74182, when used in conjunction with the SN54181 or SN74181 arithmetic logic unit (ALU), provides full high-speed carry look-ahead capability for up to n-bit words. Each SN54182/SN74182 generates the look-ahead (anticipated carry) across a group of four ALUs and, in addition, other carry look-ahead circuits may be employed to anticipate carry across sections of four look-ahead packages up to n-bits. Applications data for the SN54181/SN74181 illustrates cascading of SN54182/SN74182 circuits to perform multi-level look-ahead.

Carry inputs and outputs of the SN54181/SN74181 are in their true form and the carry propagate (P) and carry generate (G) are in negated form; therefore, the carry (input, outputs, generate, and propagate) functions of the look-ahead circuit are implemented in the compatible forms. Reinterpretations of carry functions at the SN54181/SN74181 are also applicable and compatible with the look-ahead package. Logic equations are:

$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$\overline{G} = \overline{G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0}$$
$$\overline{P} = \overline{P_3P_2P_1P_0}$$

Inputs of the SN54182/SN74182 are diode-clamped to minimize transmission-line effects, and Darlington outputs are employed to improve turn-off times and reduce propagation delay times. Typically, the average carry time is 13 nanoseconds, and power dissipation is typically 180 milliwatts or 11 milliwatts per gate. The SN54182 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74182 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Interemitter voltage (see Note 2)	5.5 V
Operating free-air temperature range: SN54182 Circuits	−55°C to 125°C
SN74182 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies to each G input in conjunction with any other G input or in conjunction with any P input.

recommended operating conditions

		SN54182 MIN	SN54182 NOM	SN54182 MAX	SN74182 MIN	SN74182 NOM	SN74182 MAX	UNIT
Supply voltage V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Operating free-air temperature range, T_A		−55	25	125	0	25	70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

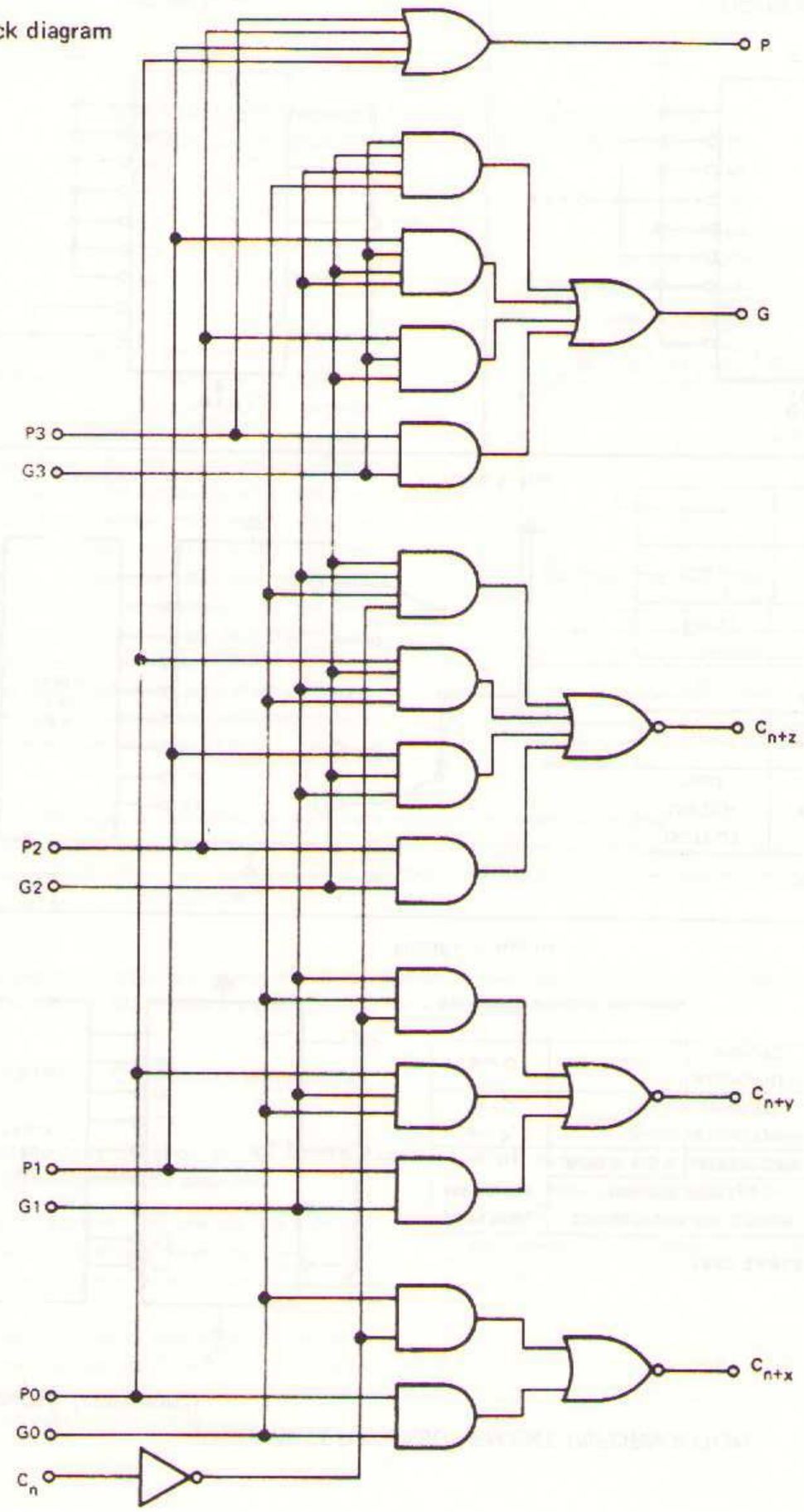
PARAMETER		TEST FIGURE	TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	1 and 2			2			V
V_{IL}	Low-level input voltage	1 and 2					0.8	V
V_{OH}	High-level output voltage	1	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = −800 μA	2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = 16 mA			0.4	V
I_{IH}	High-level input current (C_n input)	3	V_{CC} = MAX,	V_I = 2.4 V			80	μA
I_{IH}	High-level input current (P3 input)						120	μA
I_{IH}	High-level input current (P2 input)						160	μA
I_{IH}	High-level input current (P0, P1, or G3 input)						200	μA
I_{IH}	High-level input current (G0 or G2 input)						360	μA
I_{IH}	High-level input current (G1 input)						400	μA
I_{IH}	High-level input current (any input)	3	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IL}	Low-level input current (C_n input)	3	V_{CC} = MAX,	V_I = 0.4 V			−3.2	mA
I_{IL}	Low-level input current (P3 input)						−4.8	mA
I_{IL}	Low-level input current (P2 input)						−6.4	mA
I_{IL}	Low-level input current (P0, P1, or G3 input)						−8	mA
I_{IL}	Low-level input current (G0 or G2 input)						−14.4	mA
I_{IL}	Low-level input current (G1 input)						−16	mA
I_{OS}	Short-circuit output current§	4	V_{CC} = MAX		−40		−100	mA
I_{CCH}	Supply current, all outputs high	5	V_{CC} = MAX	SN54182		27		mA
				SN74182		27		
I_{CCL}	Supply current, all outputs low	6	V_{CC} = MAX	SN54182		45	65	mA
				SN74182		45	72	

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short-circuit test should not exceed 1 second.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

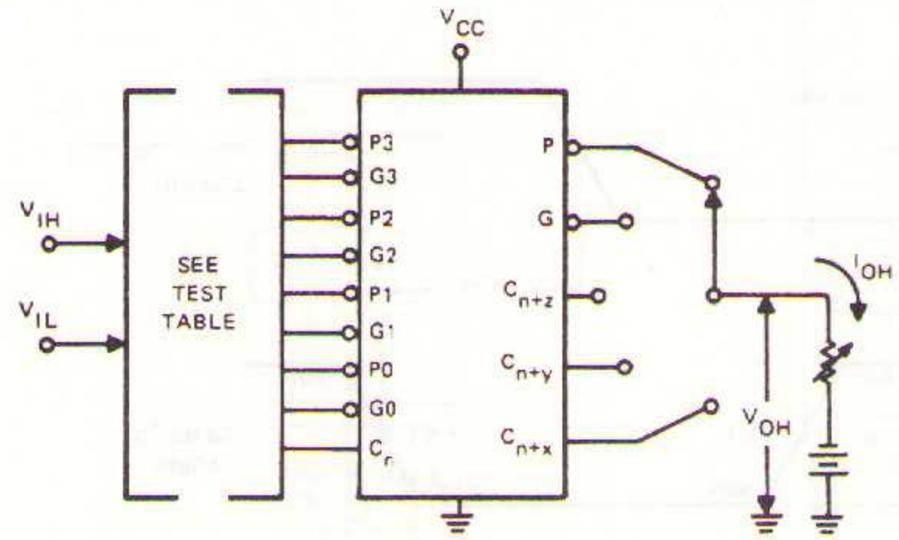
PARAMETER		TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	7	C_L = 15 pF, R_L = 400 Ω		11	17	ns
t_{PHL}	Propagation delay time, high-to-low-level output				15	22	ns

functional block diagram



PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶

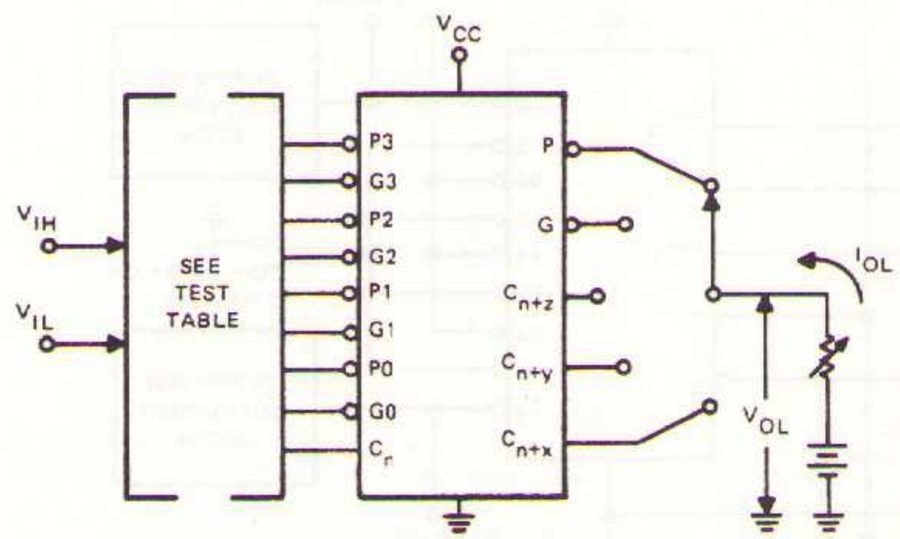


TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
P	P0	P3, P2, P1
G	P3, G3	P2, P1, G2, G1, G0
C_{n+z}	P2, P1, P0, G1, G0	G2, C_n
C_{n+y}	P1, P0, G0	G1, C_n
C_{n+x}	P0	G0, C_n

Inputs not otherwise specified are connected to ground.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



TEST TABLE

OUTPUT UNDER TEST	APPLY V_{IH}	APPLY V_{IL}
P	NONE	P3, P2, P1, P0
G	P3, P2, P1, G2, G1, P0, G0	G3
C_{n+z}	P2, G2, C_n	P1, G1, P0, G0
C_{n+y}	P1, G1, C_n	P0, G0
C_{n+x}	P0, G0, C_n	NONE

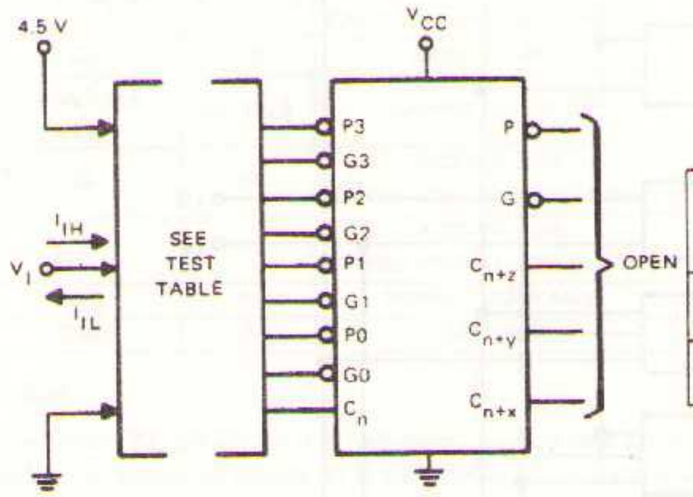
Inputs not otherwise specified are connected to ground.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}

¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

d-c test circuits§ (continued)

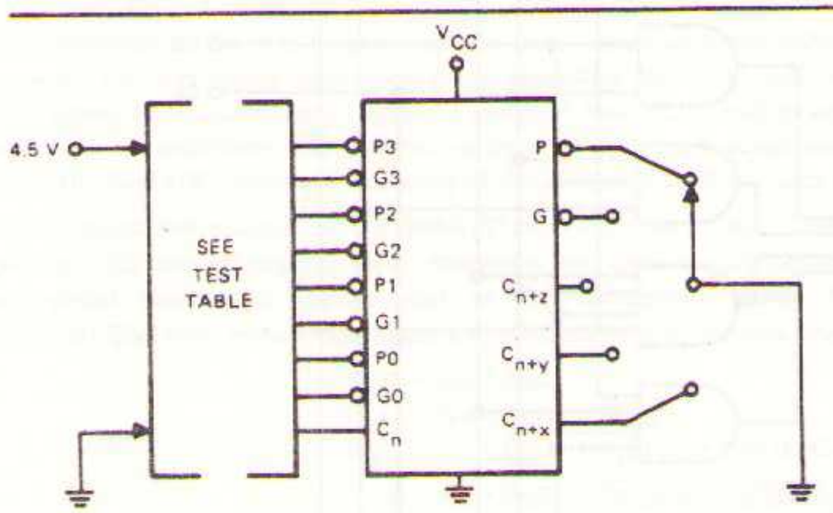


TEST TABLE

APPLY V_I, MEASURE I_{IH}, I_{IL}	CONDITIONS ON OTHER INPUTS FOR I_{IH}		CONDITIONS ON OTHER INPUTS FOR I_{IL}	
	APPLY 4.5 V	APPLY GND	APPLY 4.5 V	APPLY GND
any P, or C_n	NONE	ALL OTHER INPUTS	ALL OTHER INPUTS	NONE
any G	C_n	ALL OTHER INPUTS	ALL OTHER INPUTS	C_n

Each input is tested separately.

FIGURE 3–I_{IH}, I_{IL}



TEST TABLE

OUTPUT UNDER TEST	APPLY 4.5 V	APPLY GND
P	P3, P2, P1, P0	ALL OTHER INPUTS
G	ALL OTHER INPUTS	C_n
C_{n+z}	C_n	ALL OTHER INPUTS
C_{n+y}	C_n	ALL OTHER INPUTS
C_{n+x}	C_n	ALL OTHER INPUTS

FIGURE 4–I_{OS}

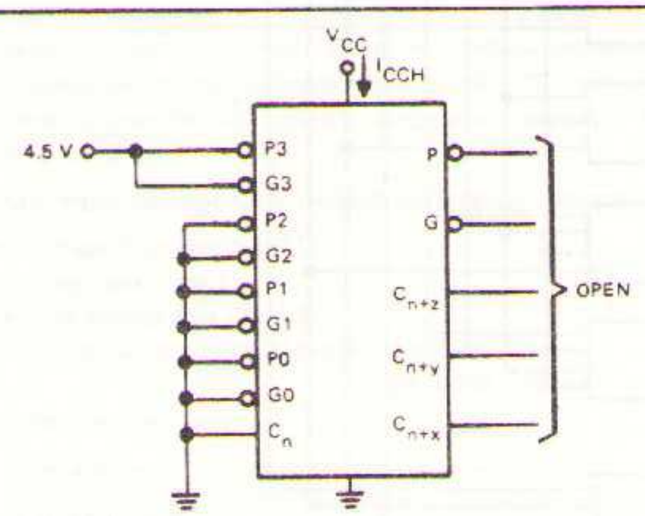


FIGURE 5–I_{CCH}

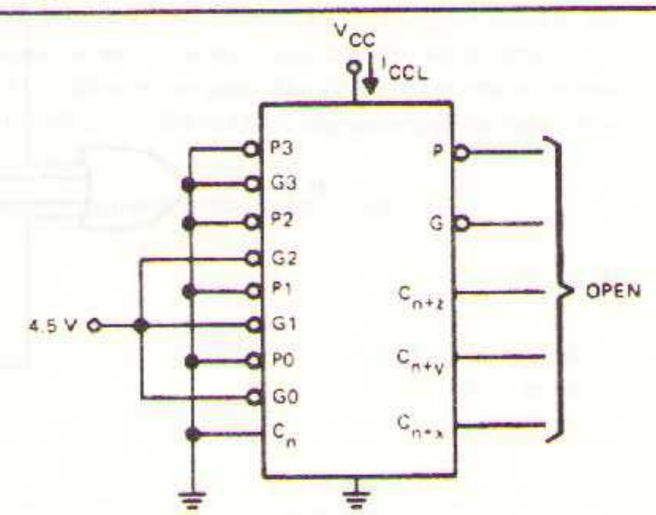
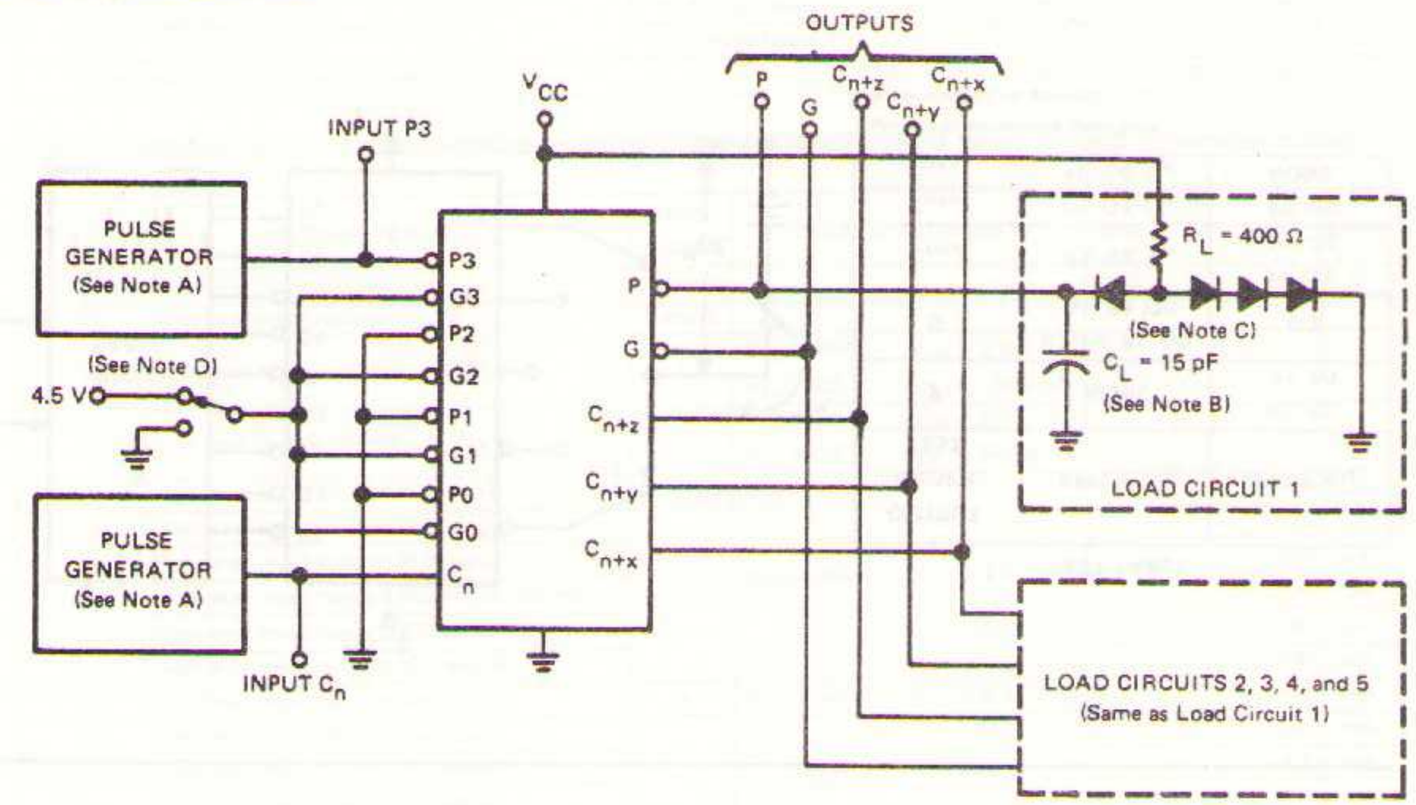


FIGURE 6–I_{CCL}

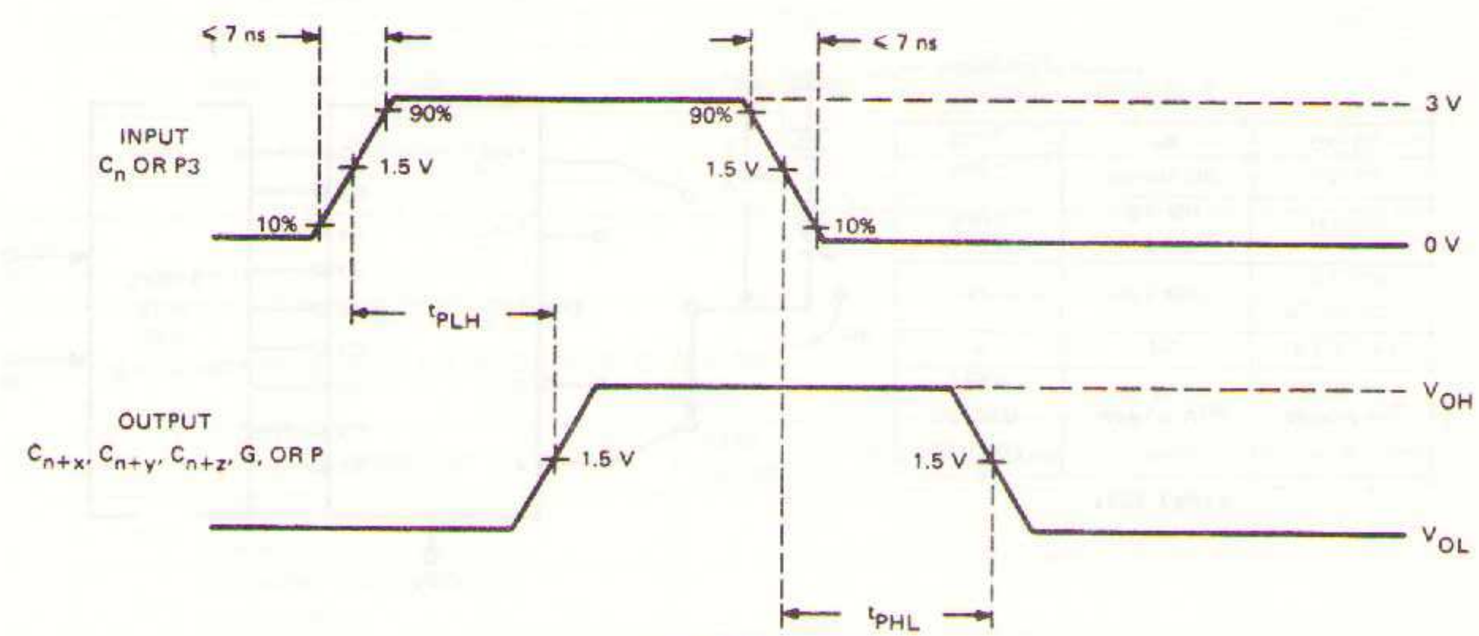
§ Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Apply 4.5 V for all tests except G output. When testing G output, apply ground.

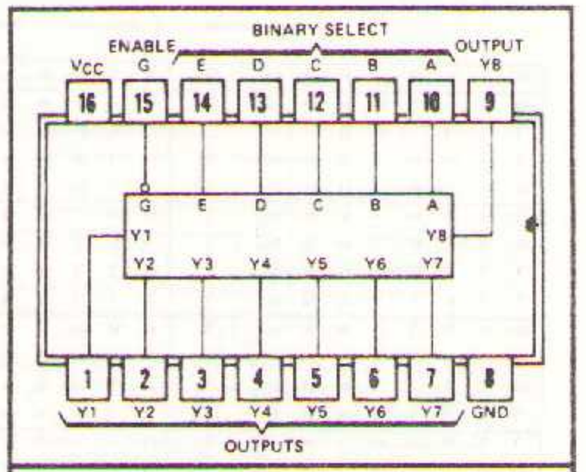
FIGURE 7–PROPAGATION DELAY TIMES

SN54184, SN74184 BCD-TO-BINARY CONVERTERS
SN54185A, SN74185A BINARY-TO-BCD CONVERTERS

description

These monolithic converters are derived from the custom MSI 256-bit read-only memories SN5488 and SN7488. Emitter connections are made to provide direct read-out of converted codes at outputs Y8 through Y1 as shown in the truth tables. These converters demonstrate the versatility of a read-only memory in that an unlimited number of reference tables or conversion tables may be built into a system using economical, customized read-only memories. Both of these converters comprehend that the least significant bits (LSB) of the binary and BCD codes are logically equal, and in each case the LSB bypasses the converter as illustrated in the typical applications. This means that a 6-bit converter is produced in each case. Both devices are cascadable to N bits.

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



positive logic: See Truth Table

†Pin assignments for these circuits are the same for all packages.

An overriding enable input is provided on each converter which, when taken high inhibits the function, causing all outputs to go high. For this reason, and to minimize power consumption, unused outputs Y7 and Y8 of the SN54185A and SN54185A, and all "don't care" conditions of the SN54184 and SN74184 are programmed high. The outputs are of the open-collector type.

The SN54184 and SN54185A are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74184 and SN74185A are characterized for operation from 0°C to 70°C.

SN54184 and SN74184 BCD-to-binary converters

The 6-bit BCD-to-binary function of the SN54184 and SN74184 is analogous to the algorithm:

a. Shift BCD number right one bit and examine each decade. Subtract three from each 4-bit decade containing a binary value greater than seven.

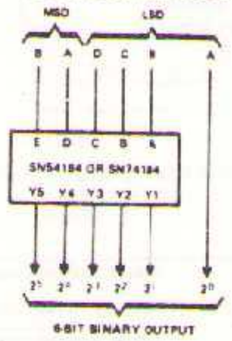
b. Shift right, examine, and correct after each shift until the least significant decade contains a number smaller than eight and all other converted decades contain zeros.

TABLE I
SN54184, SN74184
PACKAGE COUNT AND DELAY TIMES FOR BCD-TO-BINARY CONVERSION

INPUT (DECADES)	PACKAGES REQUIRED	TOTAL DELAY TIMES (ns)	
		TYP	MAX
2	2	50	80
3	6	125	200
4	11	175	280
5	19	250	400
6	28	325	520

SN54184 and SN74184 BCD-to-binary converters (continued)

6-BIT CONVERTER



TRUTH TABLE
BCD-TO-BINARY CONVERTER

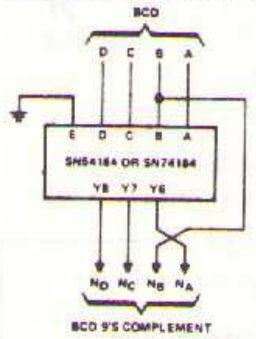
BCD WORDS	INPUTS (See Note A)						OUTPUTS (See Note B)				
	E	D	C	B	A	G	Y5	Y4	Y3	Y2	Y1
0-1	L	L	L	L	L	L	L	L	L	L	L
2-3	L	L	L	L	H	L	L	L	L	L	H
4-5	L	L	L	H	L	L	L	L	L	H	L
6-7	L	L	L	H	H	L	L	L	L	H	H
8-9	L	L	H	L	L	L	L	L	H	L	L
10-11	L	H	L	L	L	L	L	L	H	L	H
12-13	L	H	L	L	H	L	L	L	H	H	L
14-15	L	H	L	H	L	L	L	L	H	H	H
16-17	L	H	L	H	H	L	L	H	L	L	L
18-19	L	H	H	L	L	L	L	H	L	L	H
20-21	H	L	L	L	L	L	L	H	L	H	L
22-23	H	L	L	L	H	L	L	H	L	H	H
24-25	H	L	L	H	L	L	L	H	H	L	L
26-27	H	L	L	H	H	L	L	H	H	L	H
28-29	H	L	H	L	L	L	L	H	H	H	L
30-31	H	H	L	L	L	L	L	H	H	H	H
32-33	H	H	L	L	H	L	H	L	L	L	L
34-35	H	H	L	H	L	L	H	L	L	L	H
36-37	H	H	L	H	H	L	H	L	L	H	L
38-39	H	H	H	L	L	L	H	L	L	H	H
ANY	X	X	X	X	X	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

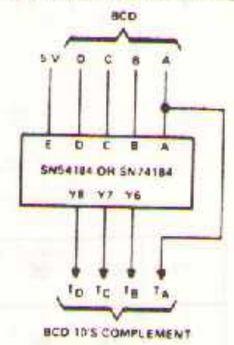
NOTES: A. Input conditions other than those shown produce highs at outputs Y1 through Y5.
B. Outputs Y6, Y7, and Y8 are not used for BCD-to-binary conversion.

In addition to BCD-to-binary conversion, the SN54184 and SN74184 are programmed to generate BCD 9's complement or BCD 10's complement. Again, in each case, one bit of the complement code is logically equal to one of the BCD bits; therefore, these complements can be produced on three lines. As outputs Y6, Y7, and Y8 are not required in the BCD-to-binary conversion, they are utilized to provide these complement codes as specified in the truth table (above, right) when the devices are connected as shown above the truth table.

BCD 9'S COMPLEMENT CONVERTER



BCD 10'S COMPLEMENT CONVERTER



TRUTH TABLE
BCD 9'S OR BCD 10'S COMPLEMENT CONVERTER

BCD WORD	INPUTS (See Note C)						OUTPUTS (See Note D)		
	E†	D	C	B	A	G	Y8	Y7	Y6
0	L	L	L	L	L	L	H	L	H
1	L	L	L	L	H	L	H	L	L
2	L	L	L	H	L	L	L	H	H
3	L	L	L	H	H	L	L	H	L
4	L	L	H	L	L	L	L	H	H
5	L	L	H	L	H	L	L	H	L
6	L	L	H	H	L	L	L	L	H
7	L	L	H	H	H	L	L	L	L
8	L	H	L	L	L	L	L	L	H
9	L	H	L	L	H	L	L	L	L
0	H	L	L	L	L	L	L	L	L
1	H	L	L	L	H	L	H	L	L
2	H	L	L	H	L	L	H	L	L
3	H	L	L	H	H	L	L	H	H
4	H	L	H	L	L	L	L	H	H
5	H	L	H	L	H	L	L	H	L
6	H	L	H	H	L	L	L	H	L
7	H	L	H	H	H	L	L	L	H
8	H	H	L	L	L	L	L	L	H
9	H	H	L	L	H	L	L	L	L
ANY	X	X	X	X	X	H	H	H	H

H = high level, L = low level, X = irrelevant

NOTES: C. Input conditions other than those shown produce highs at outputs Y6, Y7, and Y8.
D. Outputs Y1 through Y5 are not used for BCD 9's or BCD 10's complement conversion.

†When these devices are used as complement converters, input E is used as a mode control. With this input low, the BCD 9's complement is generated; when it is high, the BCD 10's complement is generated.

SN54185A and SN74185A binary-to-BCD converters

The function performed by these 6-bit binary-to-BCD converters is analogous to the algorithm:

a. Examine the three most significant bits. If the sum is greater than four, add three and shift left one bit.
b. Examine each BCD decade. If the sum is greater than four, add three and shift left one bit.
c. Repeat step b until the least-significant binary bit is in the least-significant BCD location.

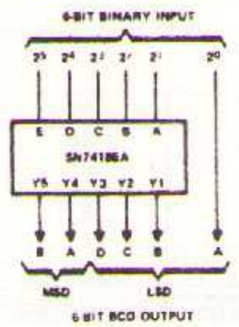
TABLE II

SN54185A, SN74185A

PACKAGE COUNT AND DELAY TIMES FOR BINARY-TO-BCD CONVERSION

INPUT (BITS)	PACKAGES REQUIRED	TOTAL DELAY TIME (ns) TYP	TOTAL DELAY TIME (ns) MAX
4 to 6	1	25	40
7 or 8	3	50	80
9	4	75	120
10	6	100	160
11	7	125	200
12	8	125	200
13	10	150	240
14	12	175	280
15	14	175	280
16	16	200	320
17	19	225	360
18	21	225	360
19	24	250	400
20	27	275	440

6-BIT CONVERTER



TRUTH TABLE

BINARY WORDS	INPUTS: BINARY SELECT E	D	C	B	A	ENABLE G	OUTPUTS: Y8	Y7	Y6	Y5	Y4	Y3	Y2	Y1
0 · 1	L	L	L	L	L	L	H	H	L	L	L	L	L	L
2 · 3	L	L	L	L	H	L	H	H	L	L	L	L	L	H
4 · 5	L	L	L	H	L	L	H	H	L	L	L	L	H	L
6 · 7	L	L	L	H	H	L	H	H	L	L	L	L	H	H
8 · 9	L	L	H	L	L	L	H	H	L	L	L	H	L	L
10 · 11	L	L	H	L	H	L	H	H	L	L	H	L	L	L
12 · 13	L	L	H	H	L	L	H	H	L	L	H	L	L	H
14 · 15	L	L	H	H	H	L	H	H	L	L	H	L	H	L
16 · 17	L	H	L	L	L	L	H	H	L	L	H	L	H	H
18 · 19	L	H	L	L	H	L	H	H	L	L	H	H	L	L
20 · 21	L	H	L	H	L	L	H	H	L	H	L	L	L	L
22 · 23	L	H	L	H	H	L	H	H	L	H	L	L	L	H
24 · 25	L	H	H	L	L	L	H	H	L	H	L	L	H	L
26 · 27	L	H	H	L	H	L	H	H	L	H	L	L	H	H
28 · 29	L	H	H	H	L	L	H	H	L	H	L	H	L	L
30 · 31	L	H	H	H	H	L	H	H	L	H	H	L	L	L
32 · 33	H	L	L	L	L	L	H	H	L	H	H	L	L	H
34 · 35	H	L	L	L	H	L	H	H	L	H	H	L	H	L
36 · 37	H	L	L	H	L	L	H	H	L	H	H	L	H	H
38 · 39	H	L	L	H	H	L	H	H	L	H	H	H	L	L
40 · 41	H	L	H	L	L	L	H	H	H	L	L	L	L	L
42 · 43	H	L	H	L	H	L	H	H	H	L	L	L	L	H
44 · 45	H	L	H	H	L	L	H	H	H	L	L	L	H	L
46 · 47	H	L	H	H	H	L	H	H	H	L	L	L	H	H
48 · 49	H	H	L	L	L	L	H	H	H	L	L	H	L	L
50 · 51	H	H	L	L	H	L	H	H	H	L	H	L	L	L
52 · 53	H	H	L	H	L	L	H	H	H	L	H	L	L	H
54 · 55	H	H	L	H	H	L	H	H	H	L	H	L	H	L
56 · 57	H	H	H	L	L	L	H	H	H	L	H	L	H	H
58 · 59	H	H	H	L	H	L	H	H	H	L	H	H	L	L
60 · 61	H	H	H	H	L	L	H	H	H	H	L	L	L	L
62 · 63	H	H	H	H	H	L	H	H	H	H	L	L	L	H
ALL	X	X	X	X	X	H	H	H	H	H	H	H	H	H

H = high level, L = low level, X = irrelevant

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 7 V
Input voltage (see Note 1) . . . . . 5.5 V
Operating free-air temperature range: SN54184, SN54185A . . . . . −55°C to 125°C
SN74184, SN74185A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

	SN54184, SN54185A MIN	NOM	MAX	SN74184, SN74185A MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Low-level output current, I_{OL}			16			16	mA
Operating free-air temperature, T_A	−55	25	125	0	25	70	°C

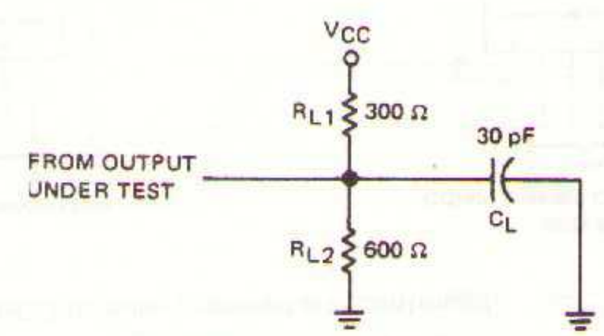
electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN,	I_I = −12 mA			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V,	V_{OH} = 5.5 V			100	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	I_{OL} = 12 mA			0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current (each input)	V_{CC} = MAX,	V_I = 2.4 V			40	μA
I_{IL}	Low-level input current (each input)	V_{CC} = MAX,	V_I = 0.4 V			−1	mA
I_{CCH}	Supply current, all outputs high	V_{CC} = MAX			50		mA
I_{CCL}	Supply current, all programmed outputs low				62	104	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from enable G	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω		16	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output from enable G			22	35	ns
t_{PLH}	Propagation delay time, low-to-high-level output from binary select			25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from binary select			20	32	ns



C_L includes probe and jig capacitance.

LOAD CIRCUIT

TYPICAL APPLICATION DATA
SN54184, SN74184

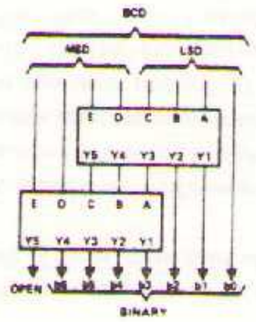


FIGURE 1–BCD-TO-BINARY CONVERTER FOR TWO BCD DECADES

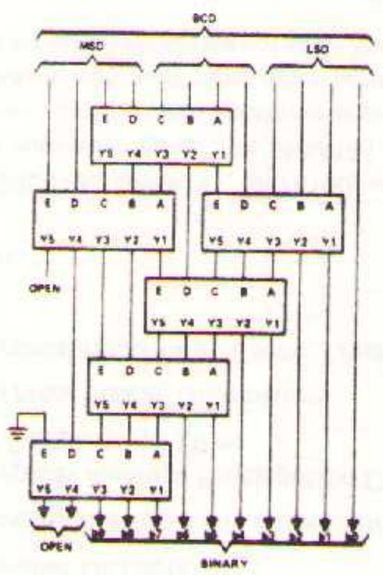


FIGURE 2–BCD-TO-BINARY CONVERTER FOR THREE BCD DECADES

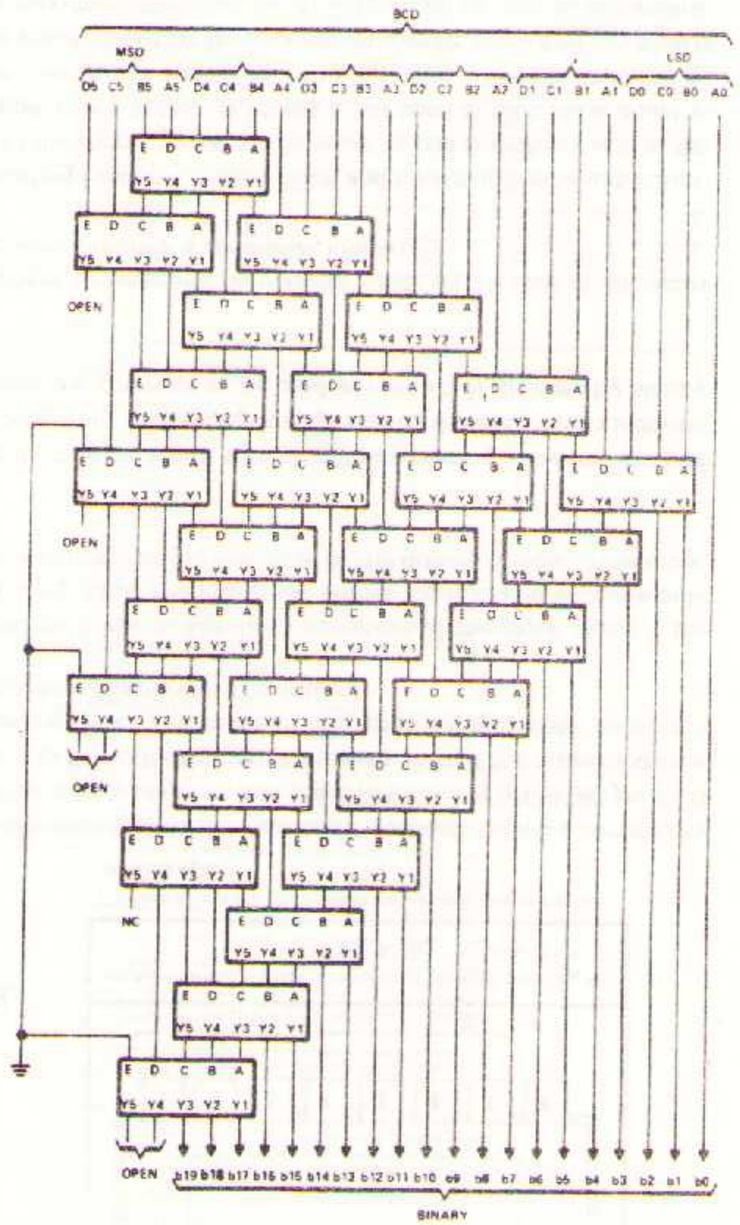


FIGURE 3–BCD-TO-BINARY CONVERTER FOR SIX BCD DECADES

MSD–most significant decade
LSD–least significant decade
Each rectangle represents an SN54184 or SN74184.

TYPICAL APPLICATION DATA
SN54185A, SN74185A

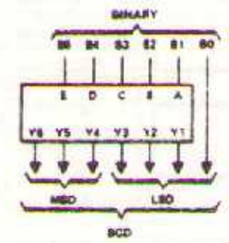


FIGURE 4–6-BIT BINARY-TO-BCD CONVERTER

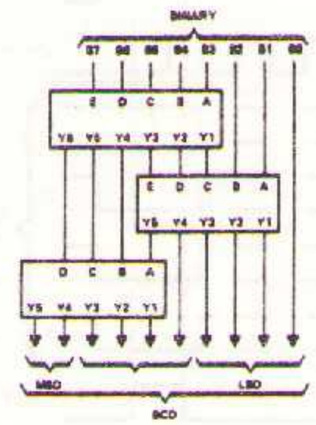


FIGURE 5–8-BIT BINARY-TO-BCD CONVERTER

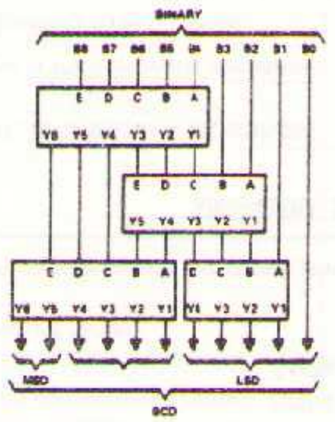


FIGURE 6–9-BIT BINARY-TO-BCD CONVERTER

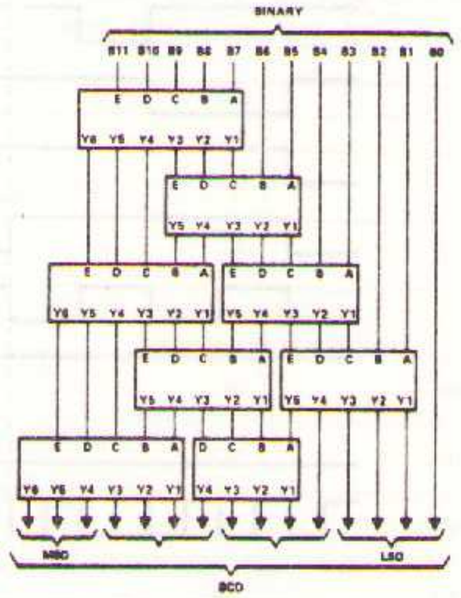


FIGURE 7–12-BIT BINARY-TO-BCD CONVERTER

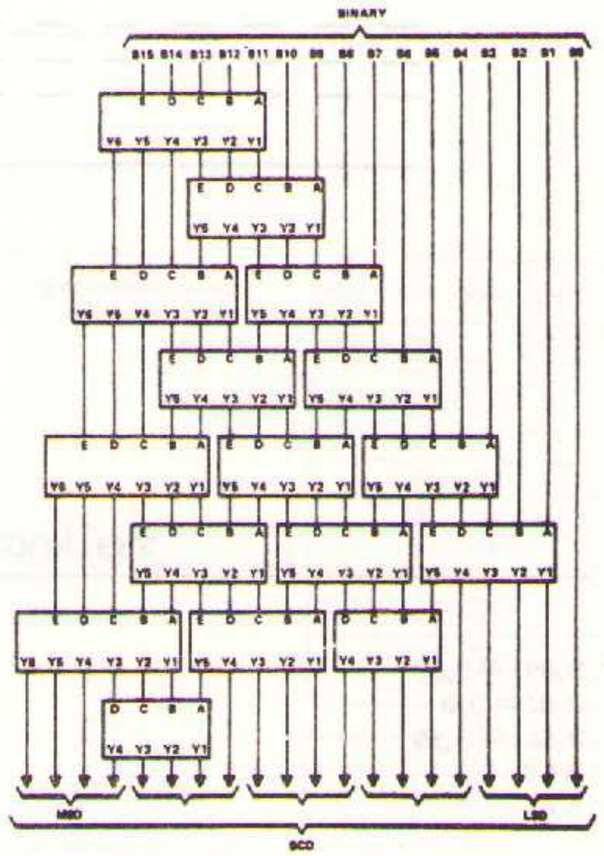
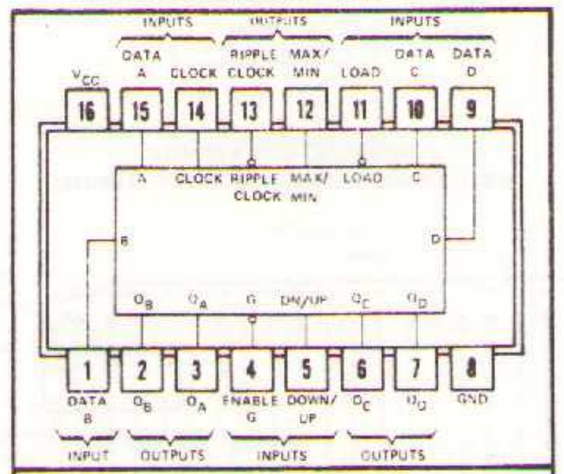


FIGURE 8–16-BIT BINARY-TO-BCD CONVERTER

MSD–Most significant decade
LSD–Least significant decade
Each rectangle represents an SN54185A or an SN74185A.

- Counts 8-4-2-1 BCD or Binary
- Single Down/Up Count Control Line
- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presettable with Load Control
- Parallel Outputs
- Cascadable for n-Bit Applications
- Typical Average Propagation Delay (Clock to Q Output) . . . 20 ns
- Typical Power Dissipation . . . 325 mW
- Typical Maximum Clock Frequency . . . 25 MHz

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



asynchronous inputs: Low input to load sets Q_A=A, Q_B = B, Q_C = C, and Q_D = D

†Pin assignments for these circuits are the same for all packages.

description

The SN54190, SN54191, SN74190, and SN74191 are synchronous, reversible up/down counters having a complexity of 58 equivalent gates. The SN54191 and SN74191 are 4-bit binary counters and the SN54190 and SN74190 are BCD counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the steering logic. This mode of operation will eliminate the output counting spikes which are normally associated with asynchronous (ripple clock) counters.

The outputs of the four master-slave flip-flops are triggered on a low-to-high-level transition of the clock input if the enable input is low. A high at the enable input inhibits counting. Level changes at the enable input should be made only when the clock input is high. The direction of the count is determined by the state of the down/up input. When low, the counter counts up and when high, it counts down.

These counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the load input and entering the desired data at the data inputs. The output will change to agree with the data inputs independently of the state of the clock input. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

Input buffers have been used to lower the fan-in requirement to only one normalized Series 54/74 load at all inputs except enable. This is important when the output of the driving circuitry is somewhat limited.

Two outputs have been made available to perform the cascading function: ripple clock and maximum/minimum count. The latter output produces a high-level output pulse with a duration approximately equal to one complete cycle of the clock when the counter overflows or underflows. The ripple clock output produces a low-level output pulse equal in width to the low-level portion of the clock input when an overflow or underflow condition exists. The counters can be easily cascaded by feeding the ripple clock output to the enable input of the succeeding counter if parallel clocking is used, or to the clock input if parallel enabling is used. The maximum/minimum count output can be used to accomplish look-ahead for high-speed operation.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input clock frequency is typically 25 megahertz and is guaranteed to be at least 20 megahertz.

The SN54190 and SN54191 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74190 and SN74191 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Operating free-air temperature range:	SN54190, SN54191	−55°C to 125°C
	SN74190, SN74191	0°C to 70°C
Storage temperature range		−65°C to 150°C

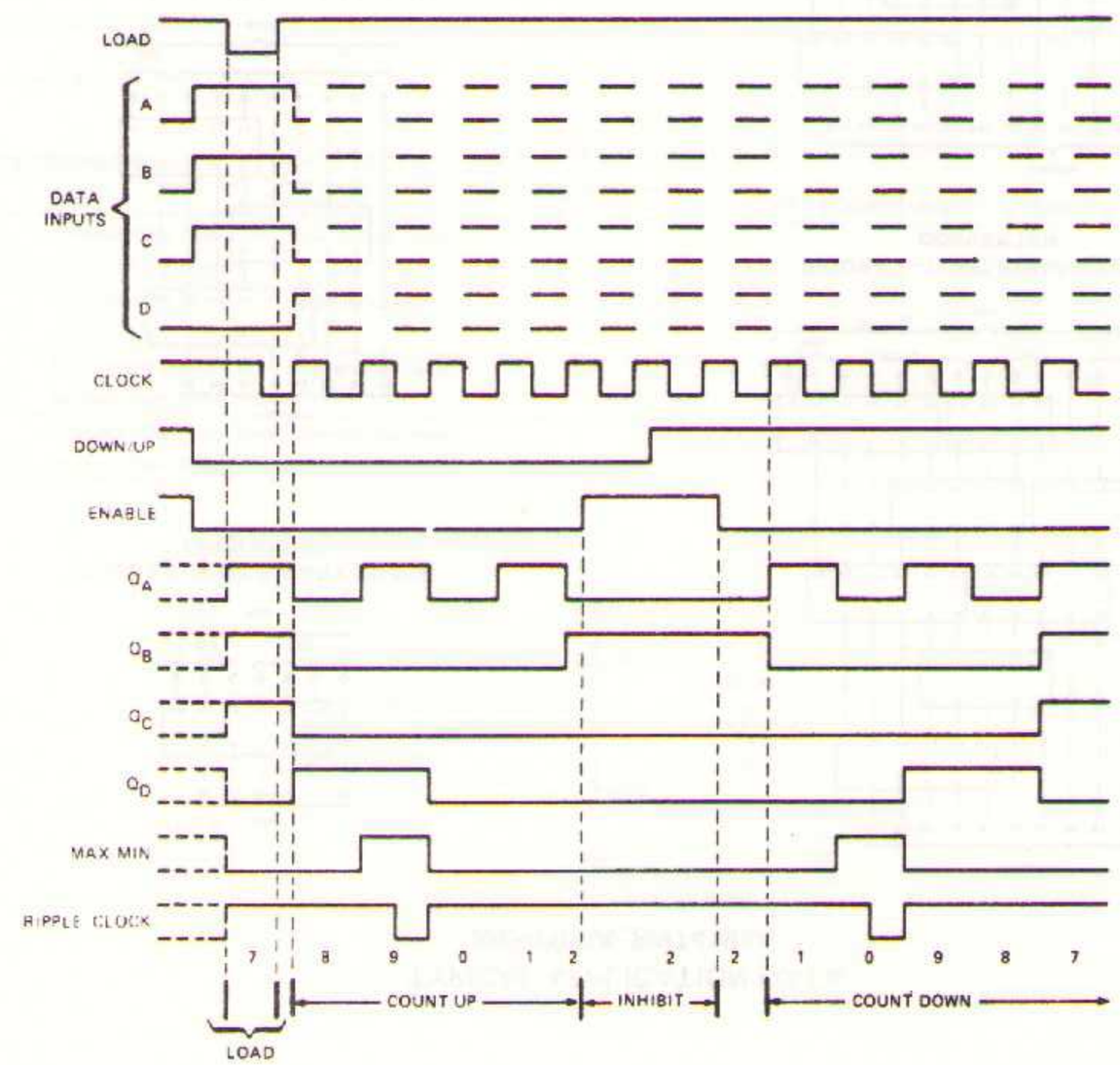
NOTE 1: Voltage values are with respect to network ground terminal.

SN54190, SN74190 DECADE COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to BCD seven.
2. Count up to eight, nine (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), nine, eight, and seven.



recommended operating conditions

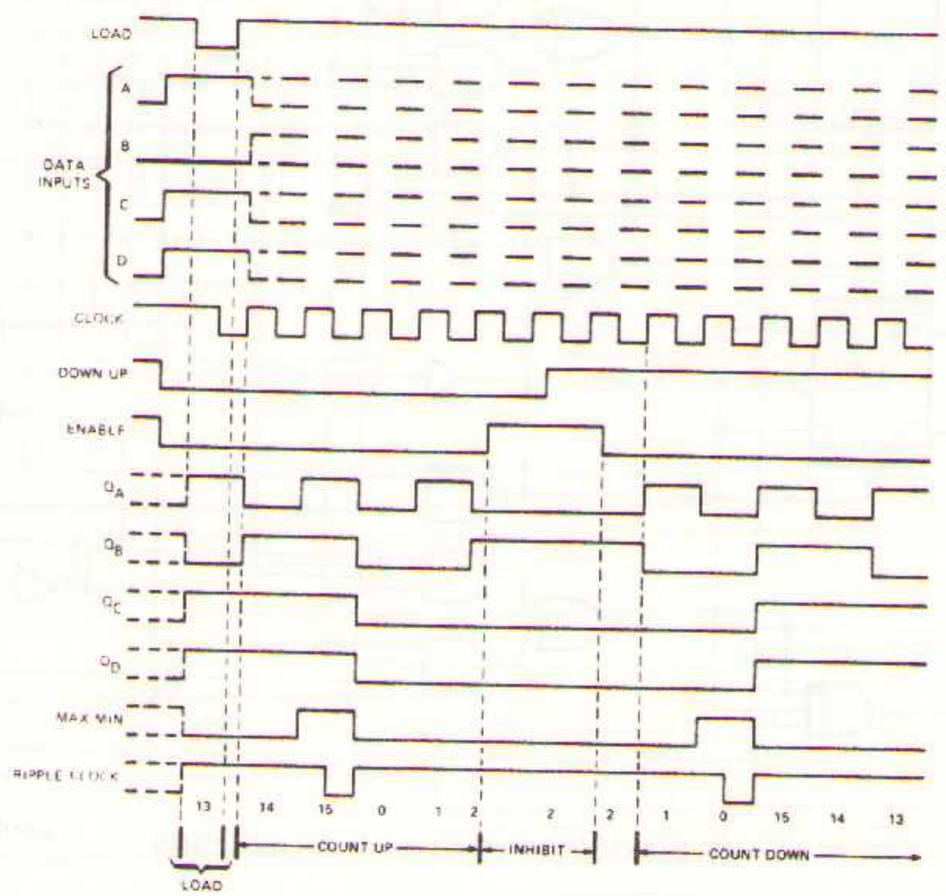
		SN54190, SN54191			SN74190, SN74191			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		20	0		20	MHz
Width of clock input pulse, $t_{w(clock)}$		25			25			ns
Width of load input pulse, $t_{w(load)}$		35			35			ns
Data setup time, t_{setup} (See Figures 1 and 2)		20			20			ns
Data hold time, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55	25	125	0	25	70	°C

SN54191, SN74191 BINARY COUNTERS

typical load, count, and inhibit sequences

Illustrated below is the following sequence:

1. Load (preset) to binary thirteen.
2. Count up to fourteen, fifteen (maximum), zero, one, and two.
3. Inhibit.
4. Count down to one, zero (minimum), fifteen, fourteen, and thirteen.



electrical characteristics over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54190, SN54191			SN74190, SN74191			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	V_{CC} = MIN	2			2			V
V_{IL}	Low-level input voltage	V_{CC} = MIN			0.8			0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_I	High-level input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current at any input except enable	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
I_{IH}	High-level input current at enable input				120			120	μA
I_{IL}	Low-level input current at any input except enable	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{IL}	Low-level input current at enable input				−4.8			−4.8	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	V_{CC} = MAX, See Note 2		65	105		65	105	mA

† For conditions shown as MAX or MIN, use appropriate value specified under recommended operating conditions for the applicable device type.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.
§ Not more than one output should be shorted at a time.
NOTE 2: I_{CC} is measured with all inputs grounded and all outputs open.

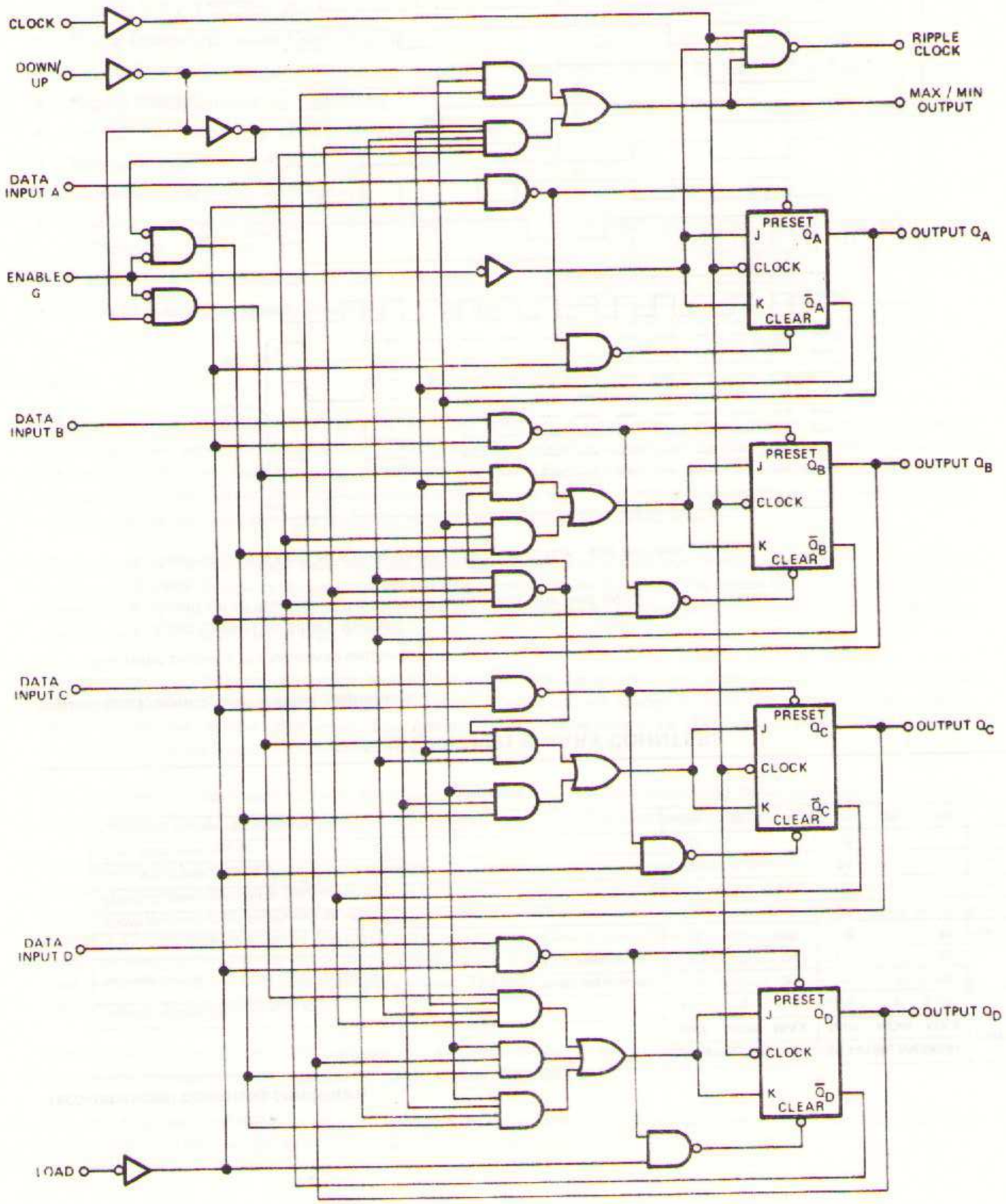
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 400 Ω, See Figure 1 and Figures 3 thru 7	20	25		MHz
t_{PLH}	Load	Q_A, Q_B, Q_C, Q_D			22	33	ns
t_{PHL}					33	50	
t_{PLH}	Data A, B, C, D	Q_A, Q_B, Q_C, Q_D			14	22	ns
t_{PHL}					35	50	
t_{PLH}	Clock	Ripple Clock			13	20	ns
t_{PHL}					16	24	
t_{PLH}	Clock	Q_A, Q_B, Q_C, Q_D			16	24	ns
t_{PHL}					24	36	
t_{PLH}	Clock	Max/Min			28	42	ns
t_{PHL}					37	52	
t_{PLH}	Down/Up	Ripple Clock			30	45	ns
t_{PHL}					30	45	
t_{PLH}	Down/Up	Max/Min			21	33	ns
t_{PHL}					22	33	

¶ f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

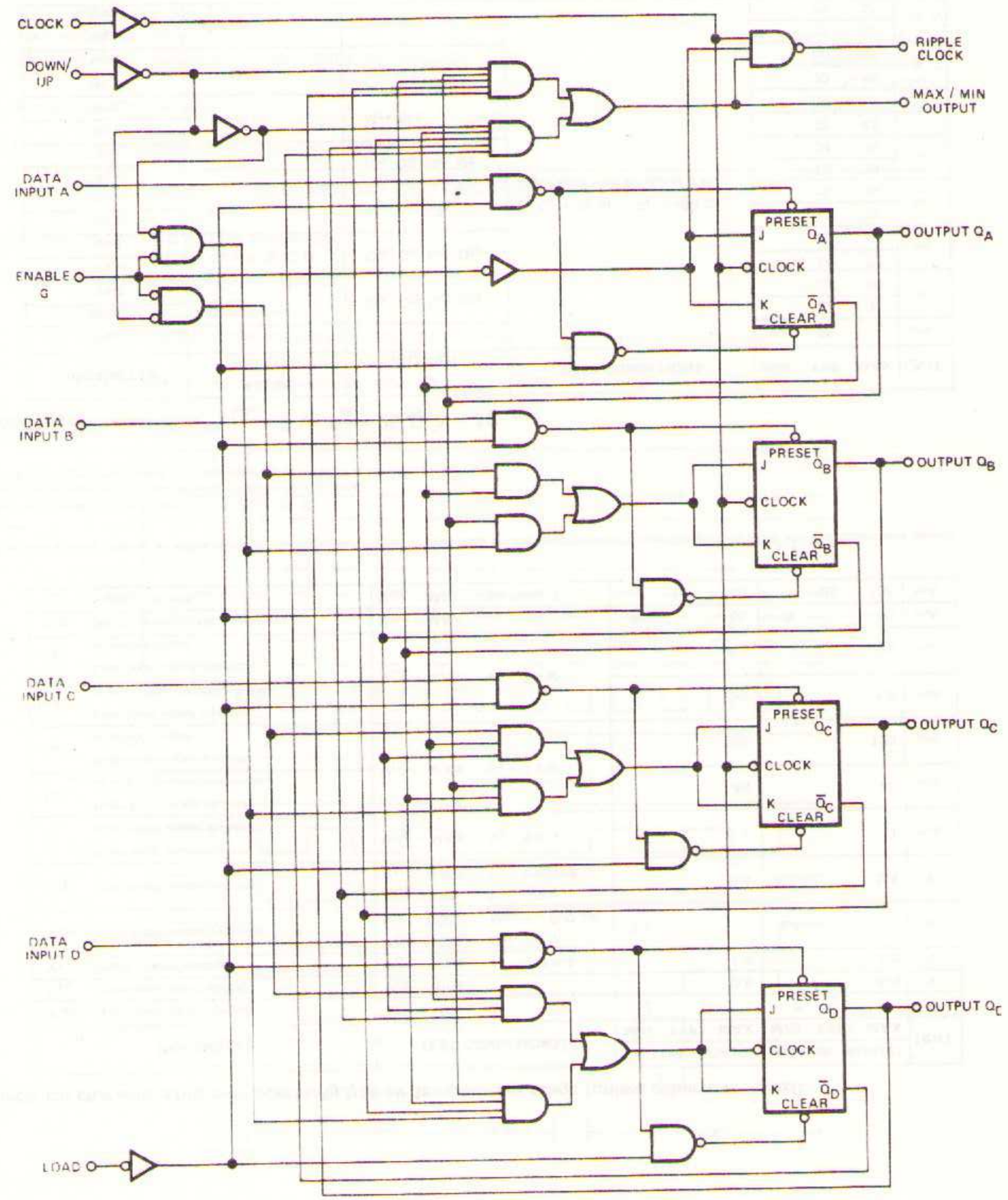
functional block diagram

SN54190, SN74190 DECADE COUNTERS



functional block diagram

SN54191, SN74191 BINARY COUNTERS



PARAMETER MEASUREMENT INFORMATION

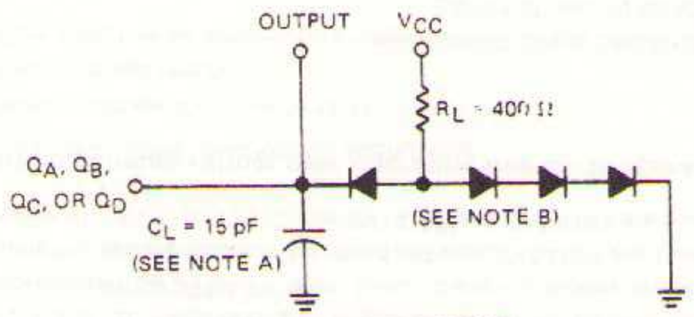


FIGURE 1—LOAD CIRCUIT FOR SWITCHING TIME MEASUREMENT

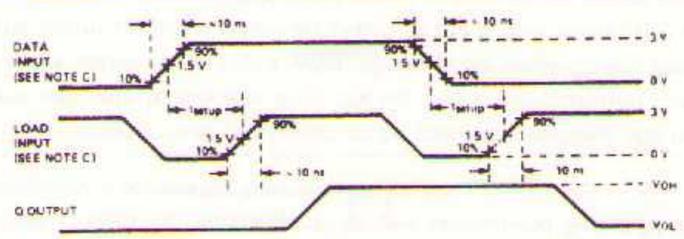
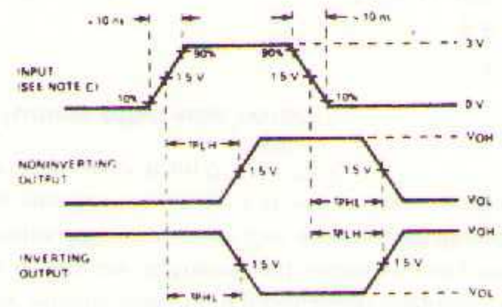


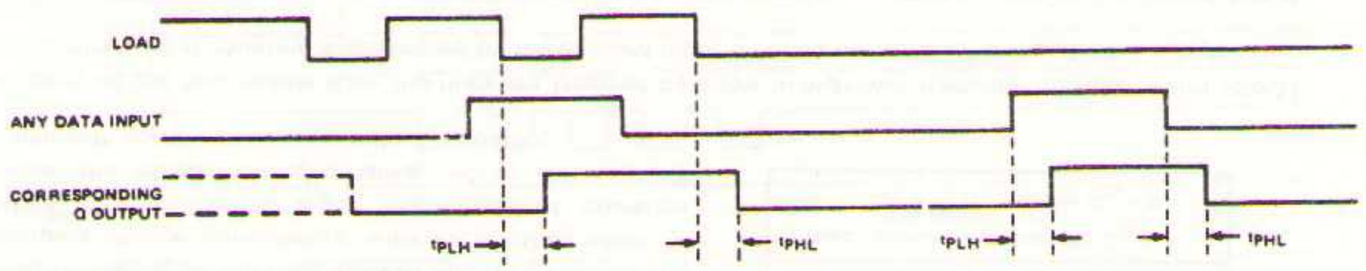
FIGURE 2—SETUP TIME VOLTAGE WAVEFORMS



See waveform sequences in figures 4 through 7 for propagation times from a specific input to a specific output. For simplification, pulse rise times, reference levels, etc., have not been shown in figures 4 through 7.

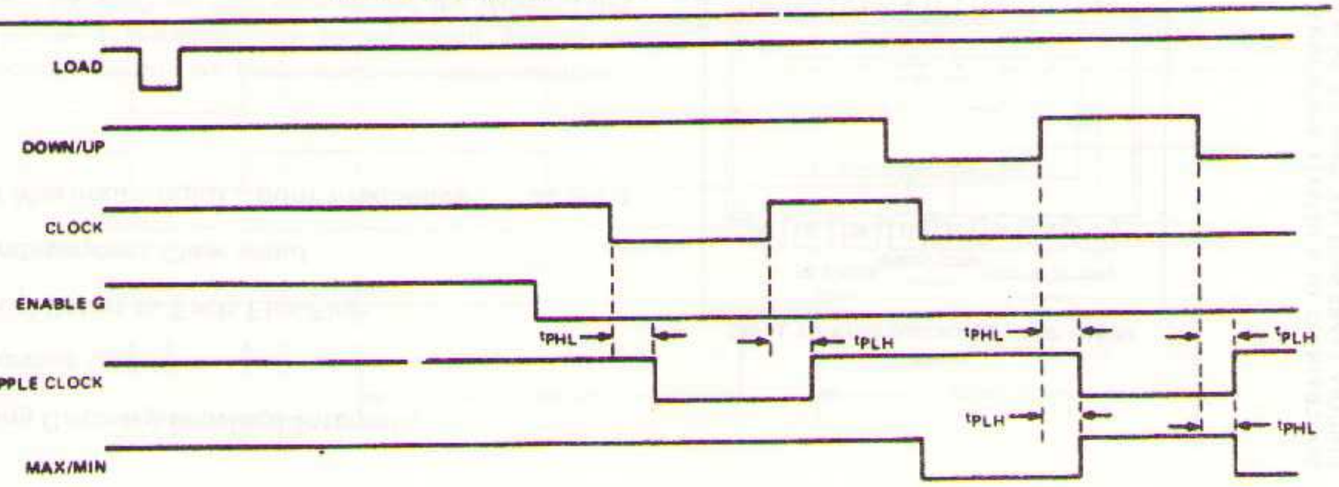
FIGURE 3—GENERAL VOLTAGE WAVEFORMS FOR PROPAGATION TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All diodes are 1N3064.
C. The input pulses are supplied by generators having the following characteristics: $Z_{out} \approx 50\ \Omega$, duty cycle ≈ 50%, PRR ≤ 1 MHz.



NOTE D: Conditions on other inputs are irrelevant.

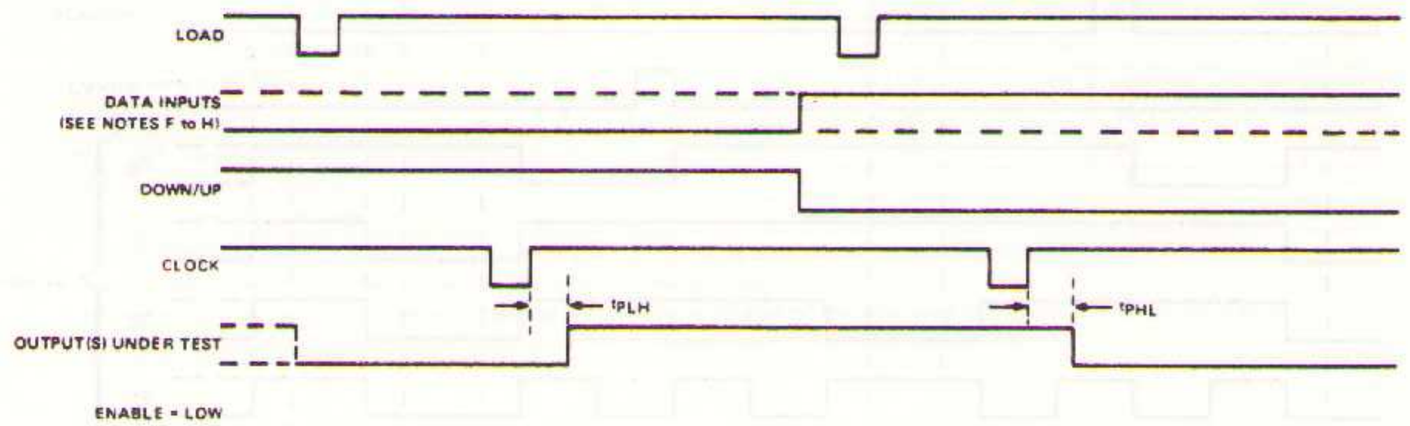
FIGURE 4—LOAD TO OUTPUT AND DATA TO OUTPUT



NOTE E: All data inputs are low.

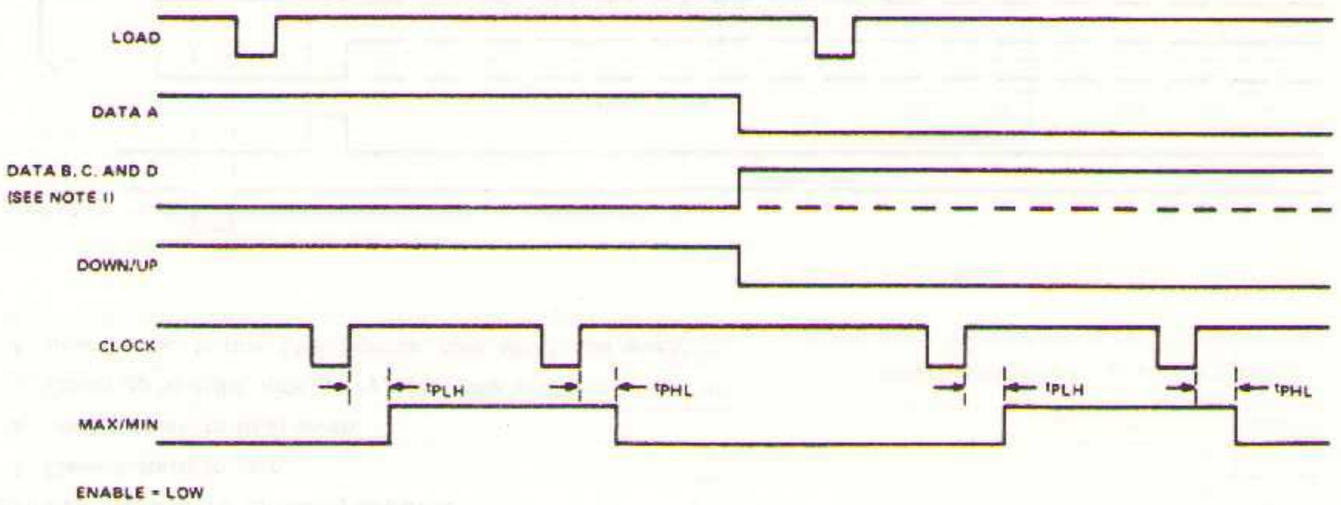
FIGURE 5—ENABLE TO RIPPLE CLOCK, CLOCK TO RIPPLE CLOCK, DOWN/UP TO RIPPLE CLOCK, AND DOWN/UP TO MAX/MIN

switching characteristics (continued)



NOTES: F. To test Q_A, Q_B, and Q_C outputs of SN54190: Data inputs A, B, and C are shown by the solid line. Data input D is shown by the dashed line.
G. To test Q_D output of SN54190: Data inputs A and D are shown by the solid line. Data inputs B and C are held at the low logic level.
H. To test Q_A, Q_B, Q_C, and Q_D outputs of SN54191: All four data inputs are shown by the solid line.

FIGURE 6—CLOCK TO OUTPUT



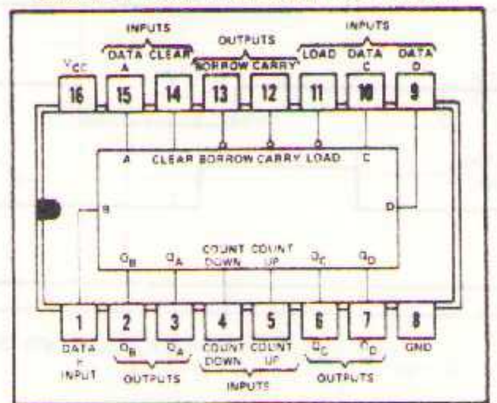
NOTE I: Data inputs B and C are shown by the dashed line for SN54190 and the solid line for SN54191. Data input D is shown by the solid line for both devices.

FIGURE 7—CLOCK TO MAX/MIN

Cascading Circuitry Provided Internally

- Synchronous Operation
- Individual Preset to Each Flip-Flop
- Fully Independent Clear Input
- Typical Maximum Input Count Frequency . . . 32 MHz

J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



logic: Low input to load sets $Q_A = A$, $Q_B = B$, $Q_C = C$, and $Q_D = D$

description

These monolithic circuits are synchronous reversible (up/down) counters having a complexity of 55 equivalent gates. The SN54192 and SN74192 are BCD counters and the SN54193 and SN74193 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincidently with each other when so instructed by the steering logic. This mode of operation eliminates the output counting spikes which are normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high-level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed while the other count input is high.

All four counters are fully programmable; that is, the outputs may be preset to any state by entering the desired data at the data inputs while the load input is low. The output will change to agree with the data inputs independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which forces all outputs to the low level when a high level is applied. The clear function is independent of the count and load inputs. An input buffer has been placed on the clear, count, and load inputs to lower the drive requirements to one normalized Series 54/74 load. This is important when the output of the driving circuitry is somewhat limited.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up- and down-counting functions. The borrow output produces a pulse equal in width to the count-down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count-up input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count-down and count-up inputs respectively of the succeeding counter.

Power dissipation is typically 325 milliwatts for either the decade or binary version. Maximum input count frequency is typically 32 megahertz and is guaranteed to be 25 MHz minimum. All inputs are buffered and represent only one normalized Series 54/74 load. Input clamping diodes are provided to minimize transmission-line effects and thereby simplify system design. The SN54192 and SN54193 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74192 and SN74193 are characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Operating free-air temperature range:	SN54192 and SN54193 Circuits	−55°C to 125°C
	SN74192 and SN74193 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

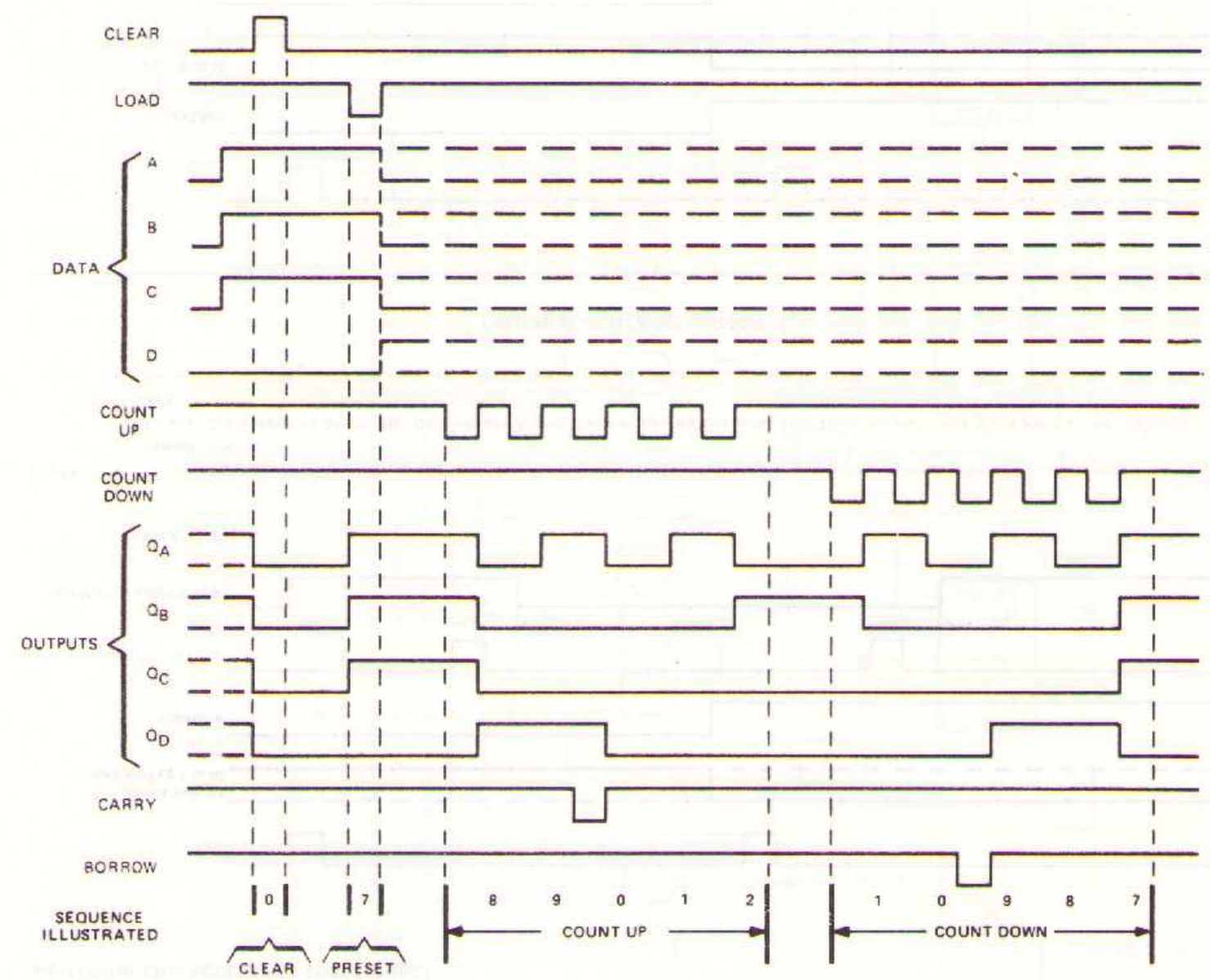
CIRCUIT TYPES SN54192, SN54193, SN74192, SN74193
BULLETIN NO. DL-S 7011311, FEBRUARY 1970

SN54192, SN74192 DECADE COUNTERS

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD seven.
3. Count up to eight, nine, carry, zero, one, and two.
4. Count down to one, zero, borrow, nine, eight, and seven.

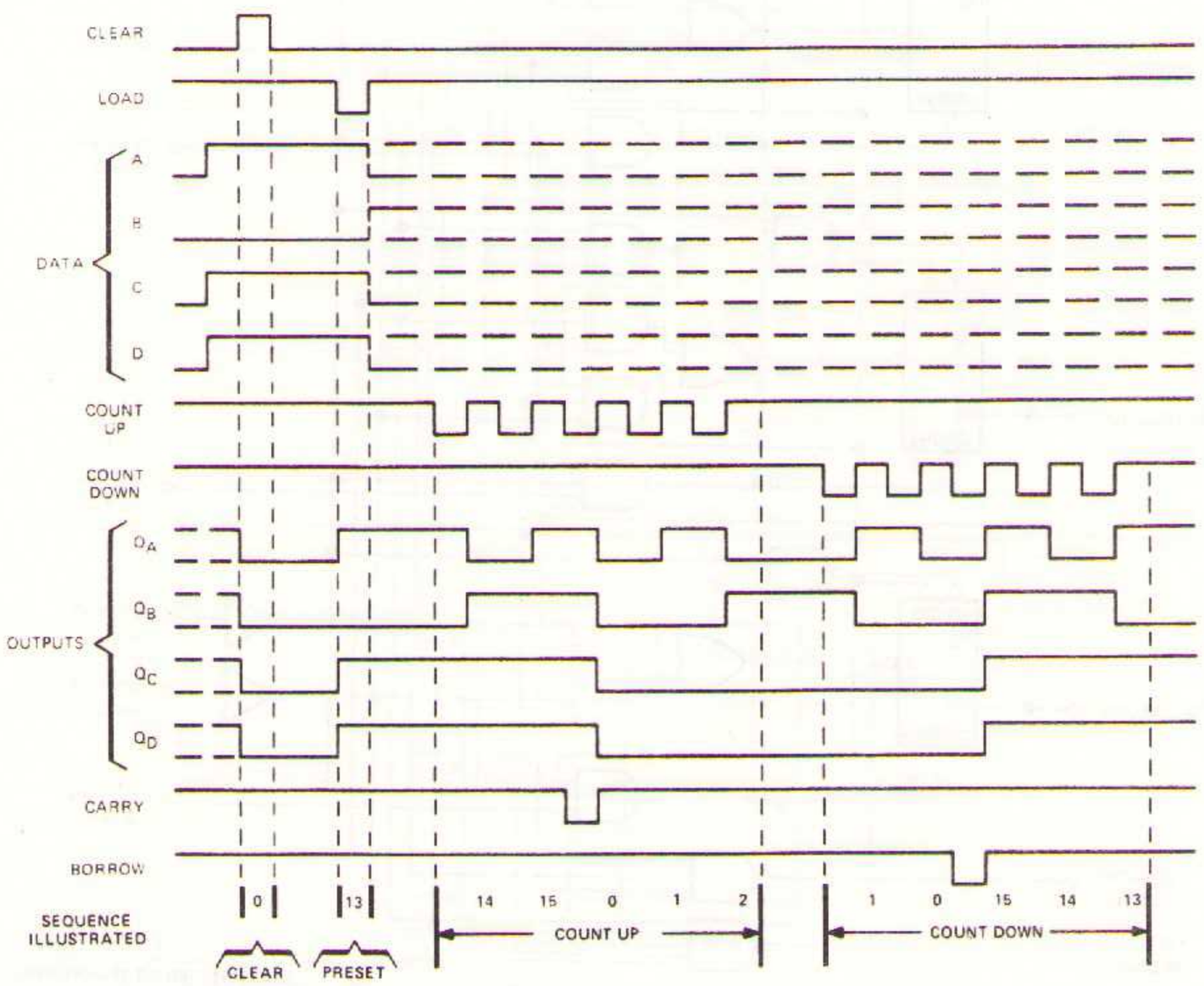


NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

typical clear, load, and count sequences

Illustrated below is the following sequence:

1. Clear outputs to zero.
2. Load (preset) to BCD thirteen.
3. Count up to fourteen, fifteen, carry, zero, one, and two.
4. Count down to one, zero, borrow, fifteen, fourteen, and thirteen.



NOTES: A. Clear overrides load, data, and count inputs.
B. When counting up, count-down input must be high; when counting down, count-up input must be high.

recommended operating conditions

	SN54192, SN54193			SN74192, SN74193			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Input count frequency, f_{count}	0		25	0		25	MHz
Width of any input pulse, t_w	20			20			ns
Data setup time, t_{setup} (see Figure 7 and Note 2)	20			20			ns
Data hold time, t_{hold} (see Note 3)	0			0			ns
Operating free-air temperature range, T_A	−55	25	125	0	25	70	C

NOTES: 2. Setup time is the interval immediately preceding the positive-going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
3. Hold time is the interval immediately following the positive going edge of the load pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST FIGURE	TEST CONDITIONS†	SN54192, SN54193			SN74192, SN74193			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage	1 and 2		2			2			V
V_{IL}	Low-level input voltage	1 and 2				0.8			0.8	V
V_{OH}	High level output voltage	1	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −400 μA	2.4			2.4			V
V_{OL}	Low-level output voltage	2	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA			0.4			0.4	V
I_{IH}	High-level input current	3	V_{CC} = MAX, V_I = 2.4 V			40			40	μA
			V_{CC} = MAX, V_I = 5.5 V			1			1	mA
I_{IL}	Low-level input current	4	V_{CC} = MAX, V_I = 0.4 V			−1.6			−1.6	mA
I_{OS}	Short-circuit output current§	5	V_{CC} = MAX	−20		−65	−18		−65	mA
I_{CC}	Supply current	6	V_{CC} = MAX		65	89		65	102	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time.

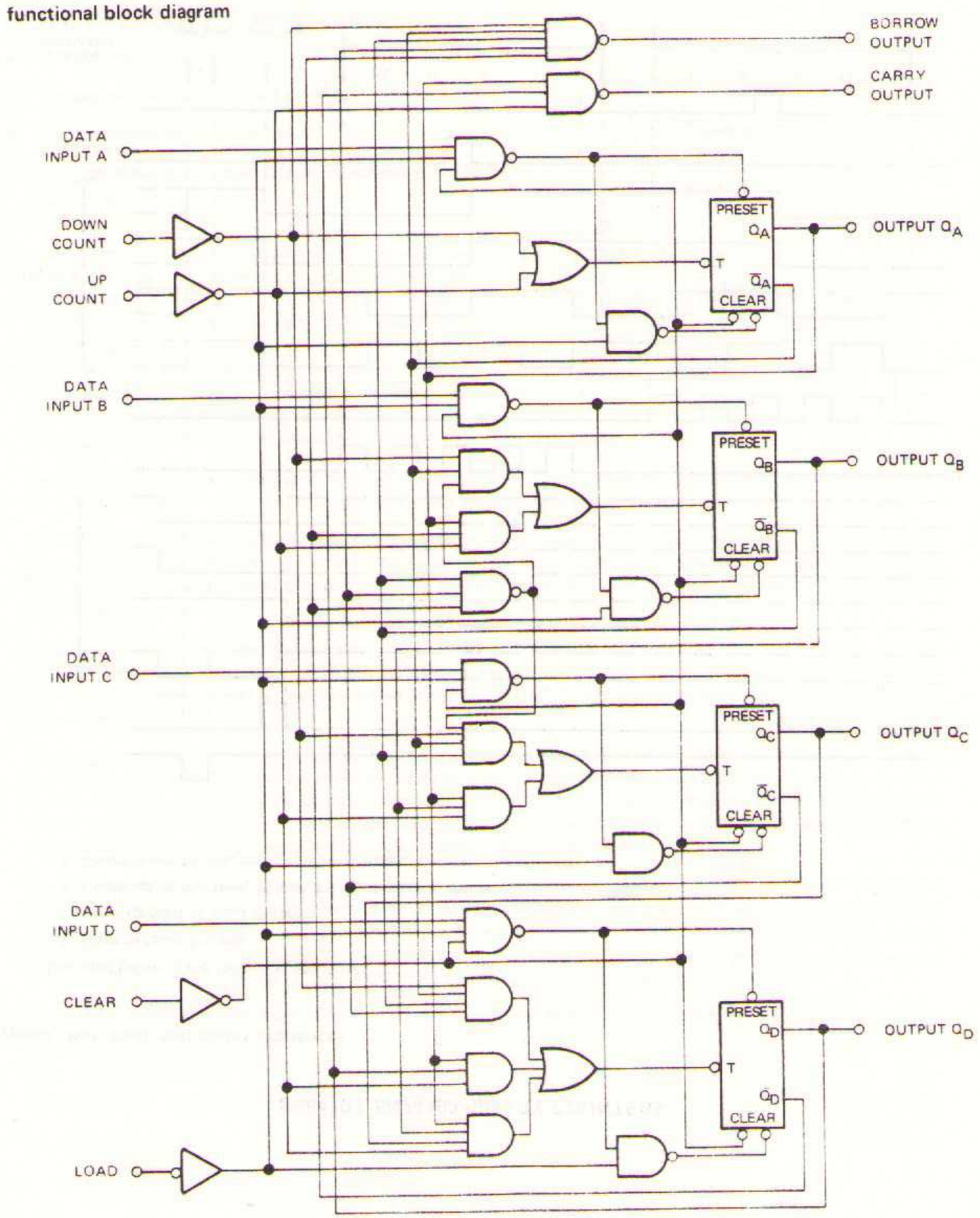
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER¶	FROM INPUT	TO OUTPUT	TEST FIGURE	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}				C_L = 15 pF, R_L = 400 Ω	25	32		MHz
t_{setup}			7			14	20	ns
t_{PLH}	Count-up	Carry	8			17	26	ns
t_{PHL}						16	24	
t_{PLH}	Count-down	Borrow	8			16	24	ns
t_{PHL}						16	24	
t_{PLH}	Either Count	Q	8			25	38	ns
t_{PHL}						31	47	
t_{PLH}	Load	Q	7			27	40	ns
t_{PLH}						29	40	
t_{PHL}	Clear	Q	7			22	35	ns

¶f_{max} = maximum clock frequency
t_{PLH} = propagation delay time, low to high-level output
t_{PHL} = propagation delay time, high to low level output

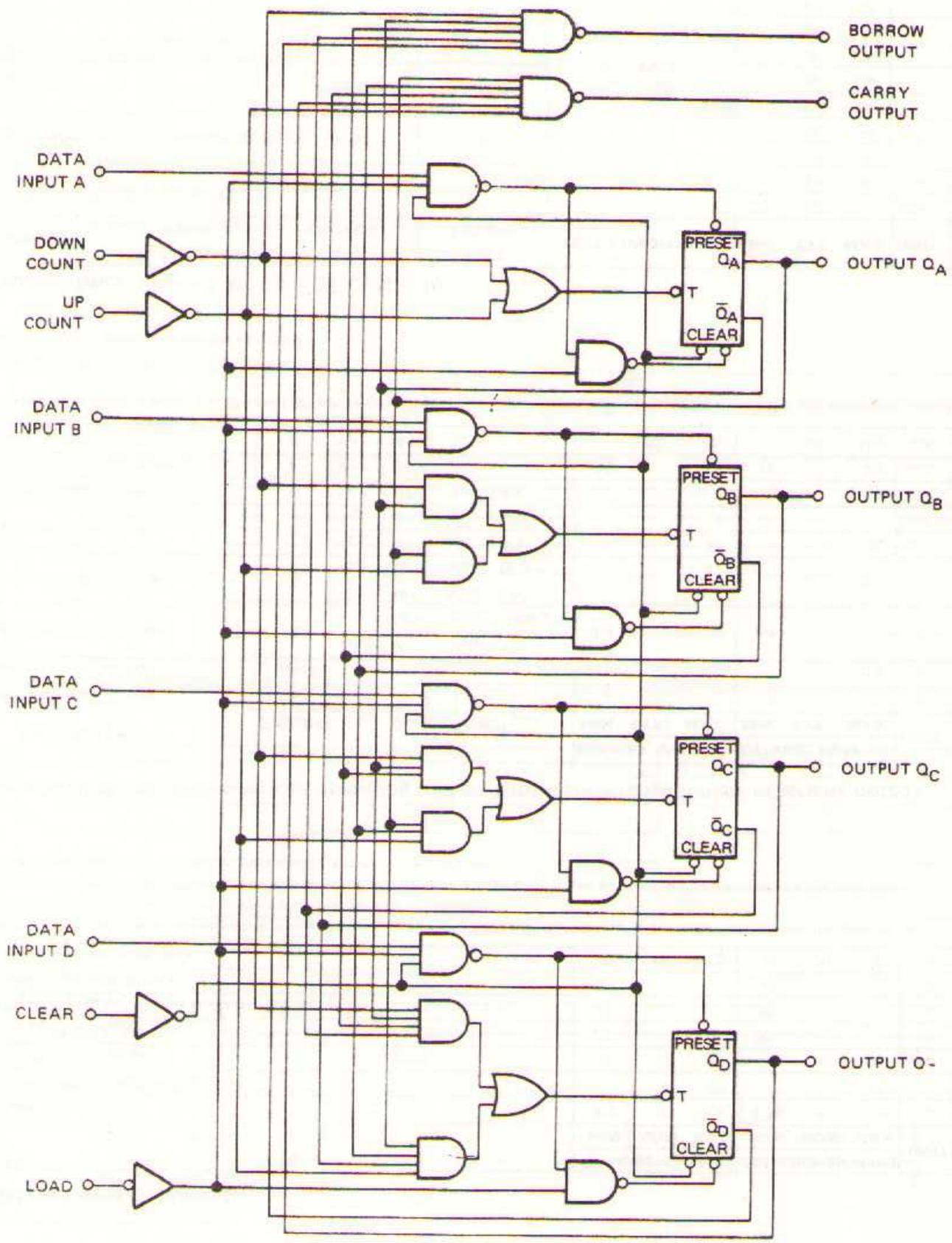
SN54192, SN74192 DECADE COUNTER

functional block diagram



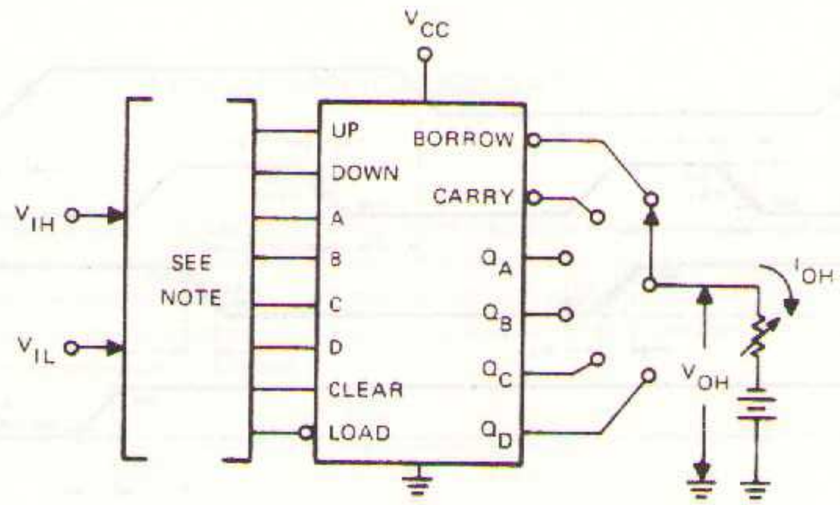
SN54193, SN74193 BINARY COUNTER

functional block diagram



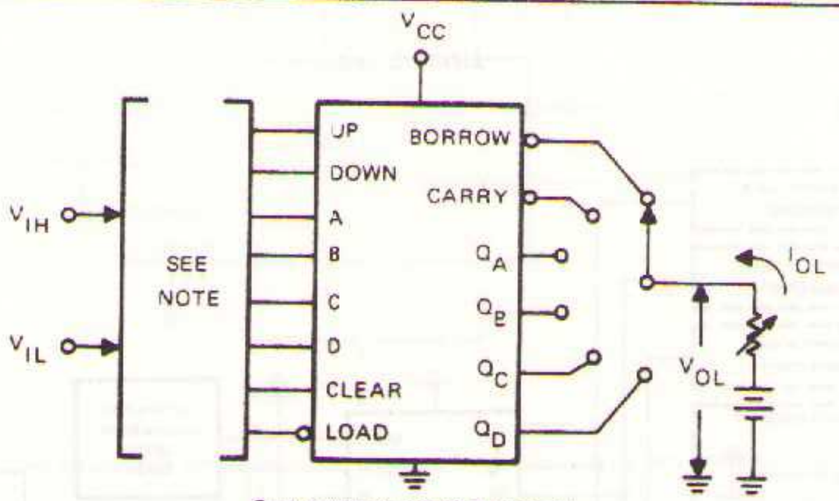
PARAMETER MEASUREMENT INFORMATION

d-c test circuits¶



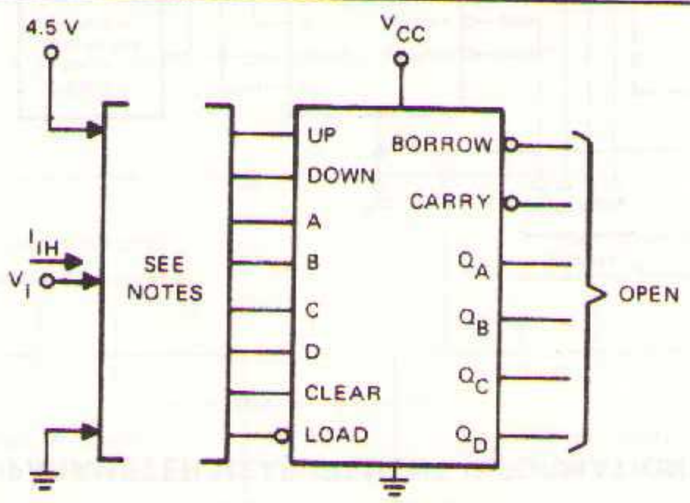
Each output is tested separately.

FIGURE 1–V_{IH}, V_{IL}, V_{OH}



Each output is tested separately.

FIGURE 2–V_{IH}, V_{IL}, V_{OL}



NOTES: A. Each input is tested separately.

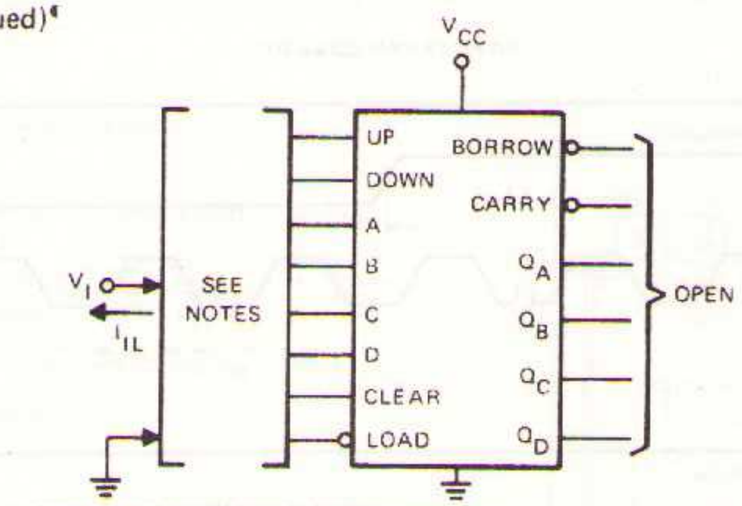
B. Apply V_I to input under test, and ground other inputs except when testing data inputs, apply 4.5 V to clear and load inputs.

FIGURE 3–I_{IH}

¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

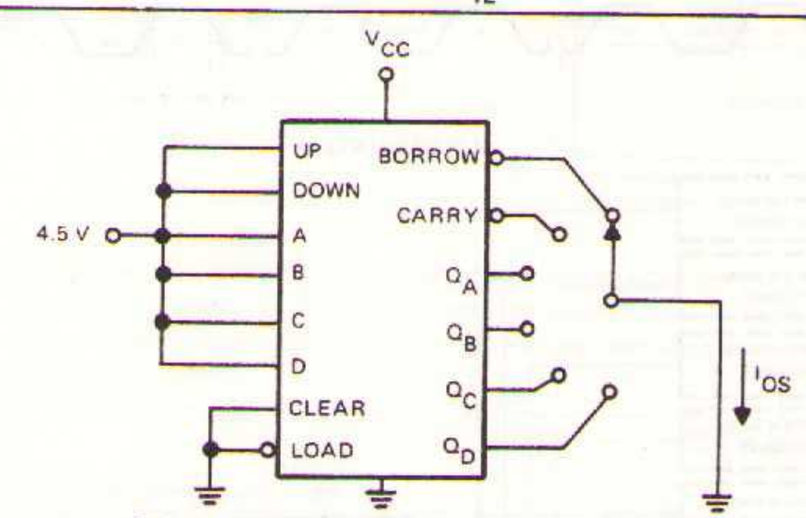
d-c test circuits (continued)¶



NOTES: A. Each input is tested separately.

B. Apply V_I to input under test and ground other inputs.

FIGURE 4–I_{IL}



Each output is tested separately in the high-level state.

FIGURE 5–I_{OS}

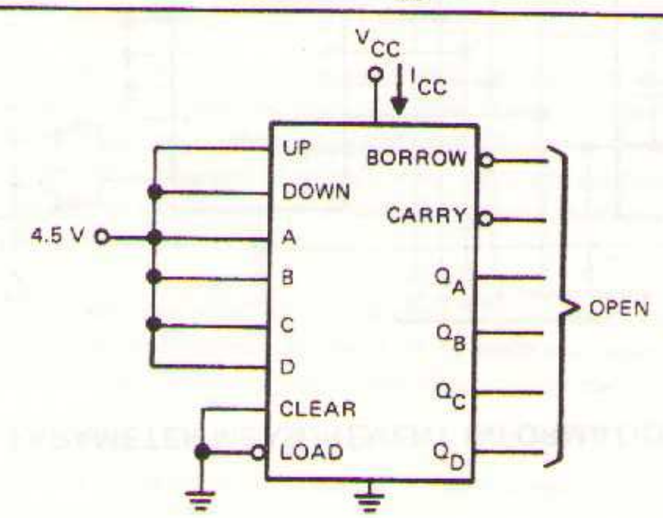
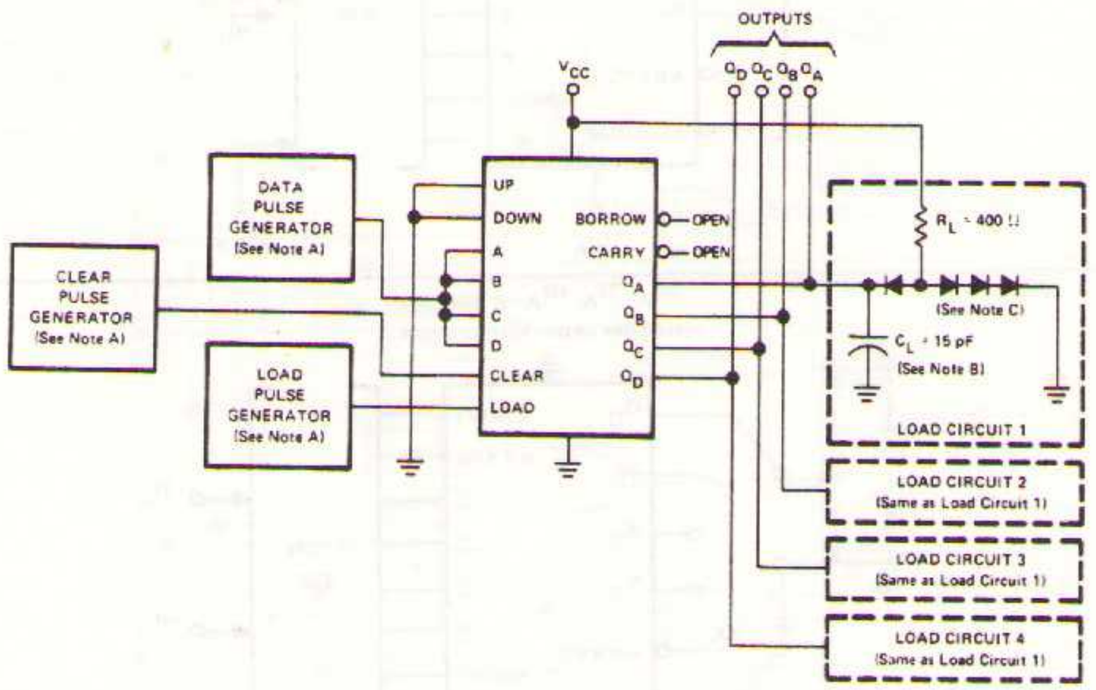


FIGURE 6–I_{CC}

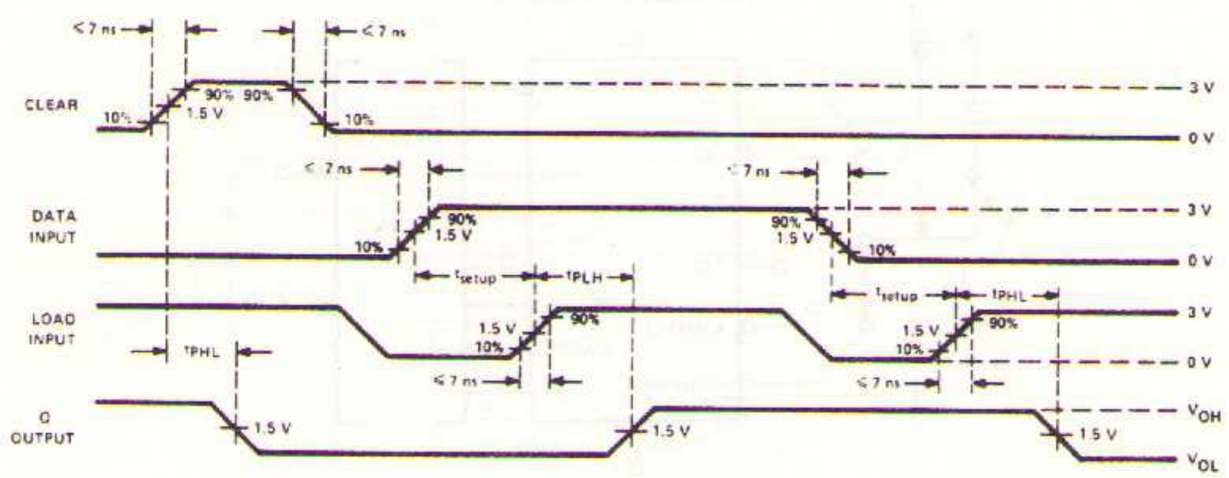
¶Arrows indicate actual direction of current flow. Current into a terminal is a positive value.

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



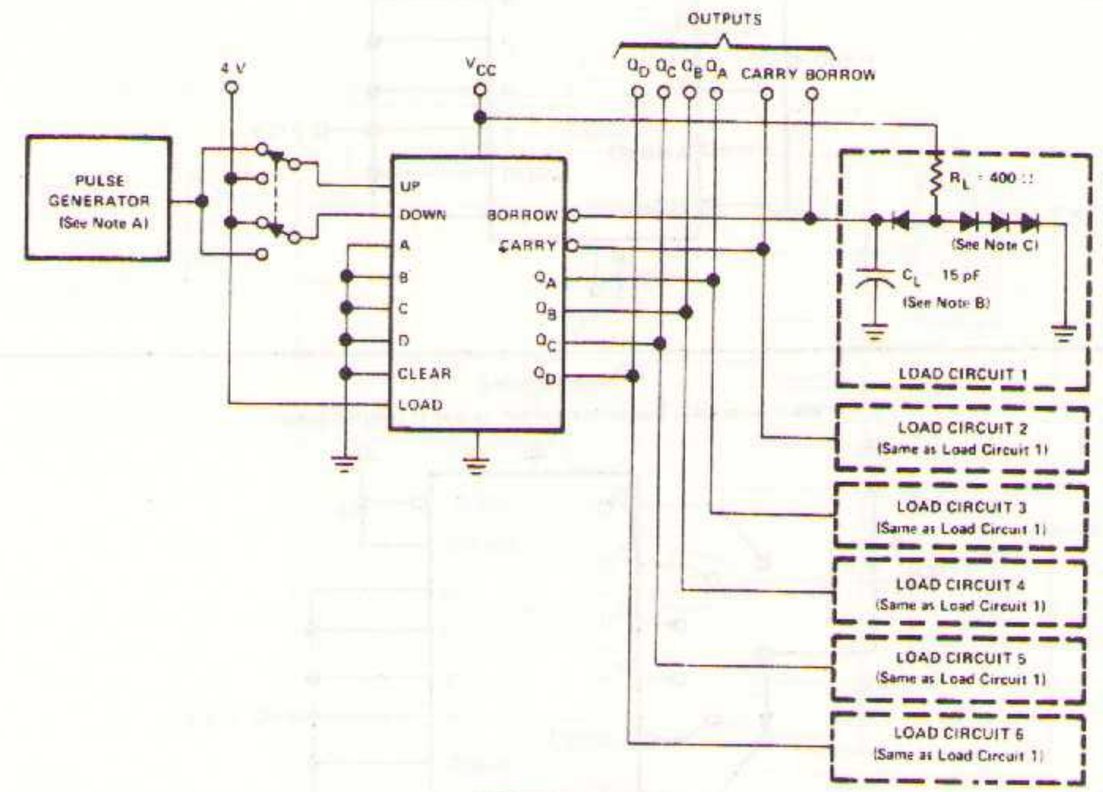
VOLTAGE WAVEFORMS

NOTES: A. The pulse generators have the following characteristics: $Z_{out} \approx 50\ \Omega$; for the data pulse generator, PRR = 500 kHz, duty cycle = 50%; for the load pulse generator, PRR = 1 MHz, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.

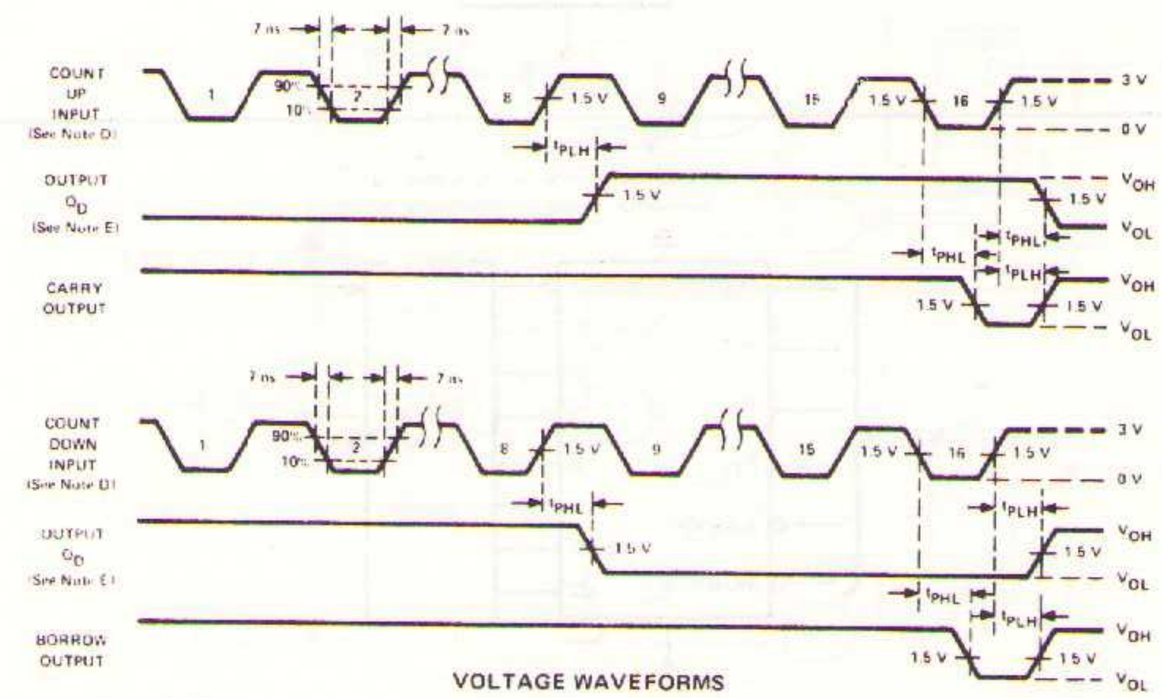
FIGURE 7–CLEAR, SETUP, AND LOAD TIMES

PARAMETER MEASUREMENT INFORMATION

switching characteristics



TEST CIRCUIT



VOLTAGE WAVEFORMS

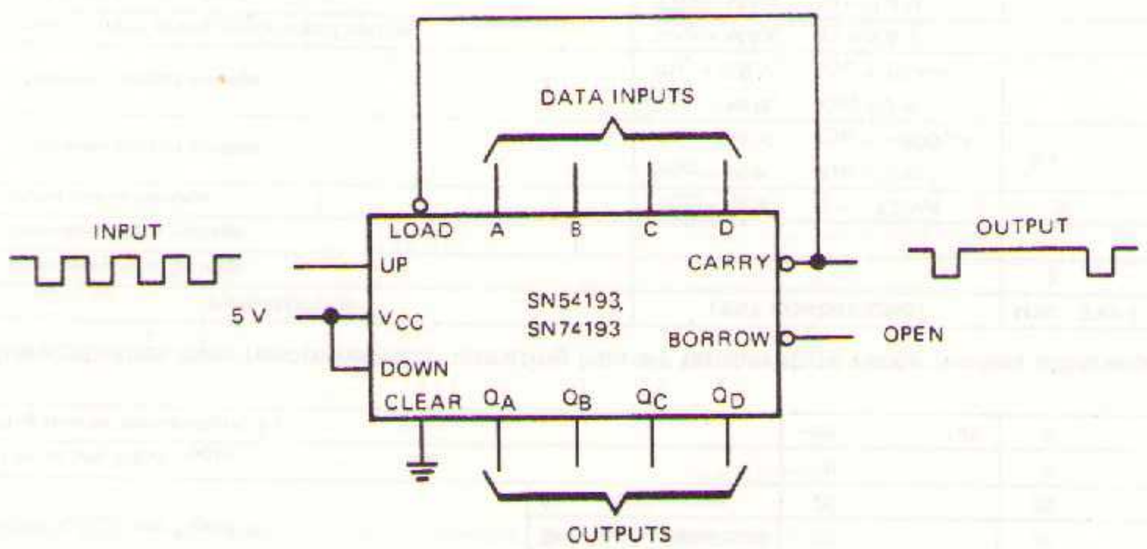
NOTES: A. The pulse generator has the following characteristics: PRR = 1 MHz, $Z_{out} \approx 50\ \Omega$, duty cycle = 50%.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N3064.
D. Count up and count-down pulses shown are for the SN54193/SN74193 binary counters. Count cycle for SN54192 decade counter is 1 through 10.
E. Waveforms for outputs Q_A, Q_B, and Q_C are omitted to simplify the drawing.

FIGURE 8–PROPAGATION DELAY TIMES

TYPICAL APPLICATION DATA

modulo-N divider

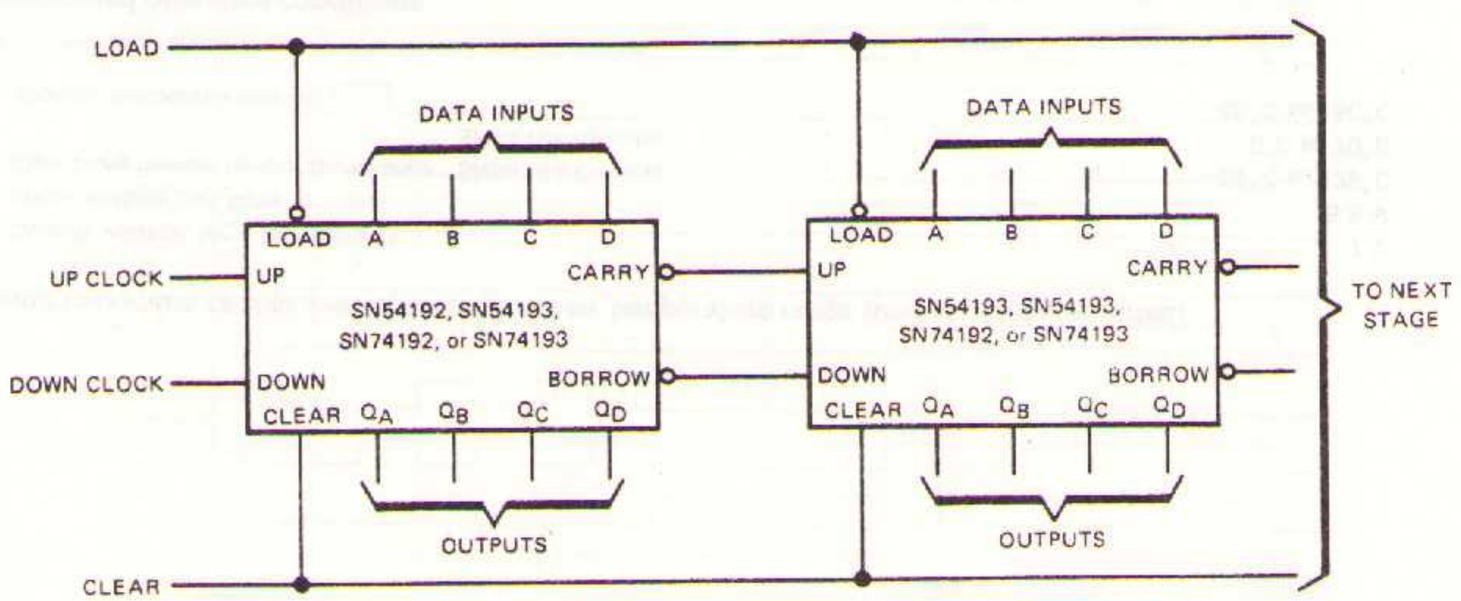
The SN54193/SN74193 can be used to divide an incoming count frequency by any integral number (N) from one to 16. This is done by modifying the count frequency occurring at the carry output by presetting the data inputs to 16 minus N. By connecting the carry output to the load input, the counter will count to the maximum state (15) and the data inputs will then be enabled on the succeeding clock pulse. The counter outputs are then preset to the levels applied at the data inputs and the count sequence is repeated.



The SN54192/SN74192 may be used in the same manner to perform division by any number from 1 to 10.

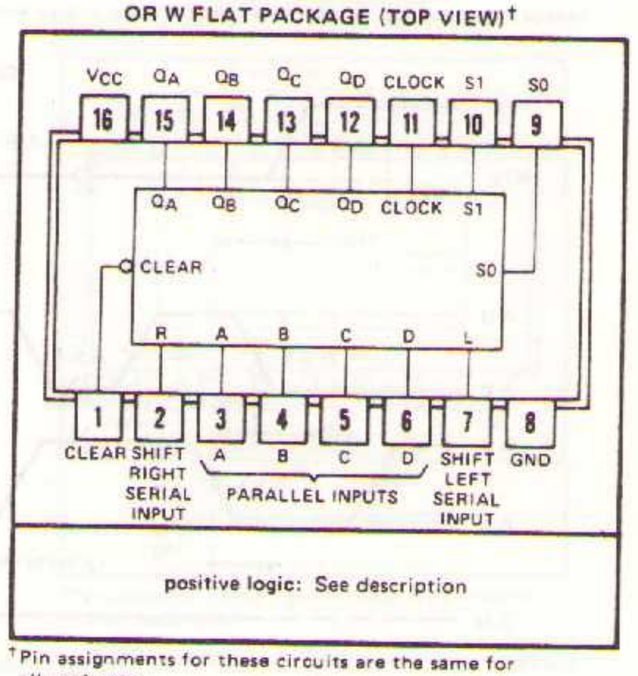
cascading

Circuitry is provided internally for cascading these counters. The mode of cascading shown below is ripple borrow/carry. No external components are required.



- Parallel Inputs and Outputs
- Four Operating Modes:
  - Synchronous Parallel Load
  - Left Shift
  - Right Shift
  - Do Nothing
- Positive Edge-Triggered Clocking
- Direct Overriding Clear

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 46 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

	MODE CONTROL	
	S1	S0
Parallel (Broadside) Load	H	H
Shift Right (In the direction Q_A toward Q_D)	L	H
Shift Left (In the direction Q_D toward Q_A)	H	L
Inhibit Clock (Do nothing)	L	L

In the parallel-load mode, data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited. Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input. Clocking of the flip-flops is inhibited when both mode-control inputs are low. The mode controls should be changed only while the clock input is high.

These four-bit shift registers are compatible with most other TTL and DTL logic families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, and input clamping diodes minimize switching transients to simplify system design. Maximum input clock frequency is typically 36 megahertz and power dissipation is typically 195 mW.

The SN54194 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74194 is characterized for operation from 0°C to 70°C.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Operating free-air temperature range:	SN54194 Circuits	−55°C to 125°C
	SN74194 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54194			SN74194			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock or clear pulse, t_w		20			20			ns
Setup time, t_{setup} (see Figure 1)	Mode control	30			30			ns
	Serial and parallel data	20			20			ns
	Clear inactive-state	25			25			ns
Hold time at any input, t_{hold}		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54194	−20		−57	mA
			SN74194	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

NOTE 2: With all outputs open, inputs A through D grounded, and 4.5 V applied to S0, S1, clear, and the serial inputs, I_{CC} is tested with a momentary ground, then 4.5 V, applied to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

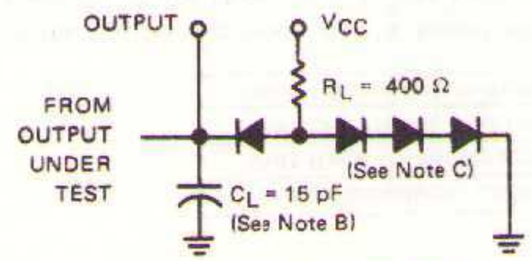
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	25	36		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		7	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	

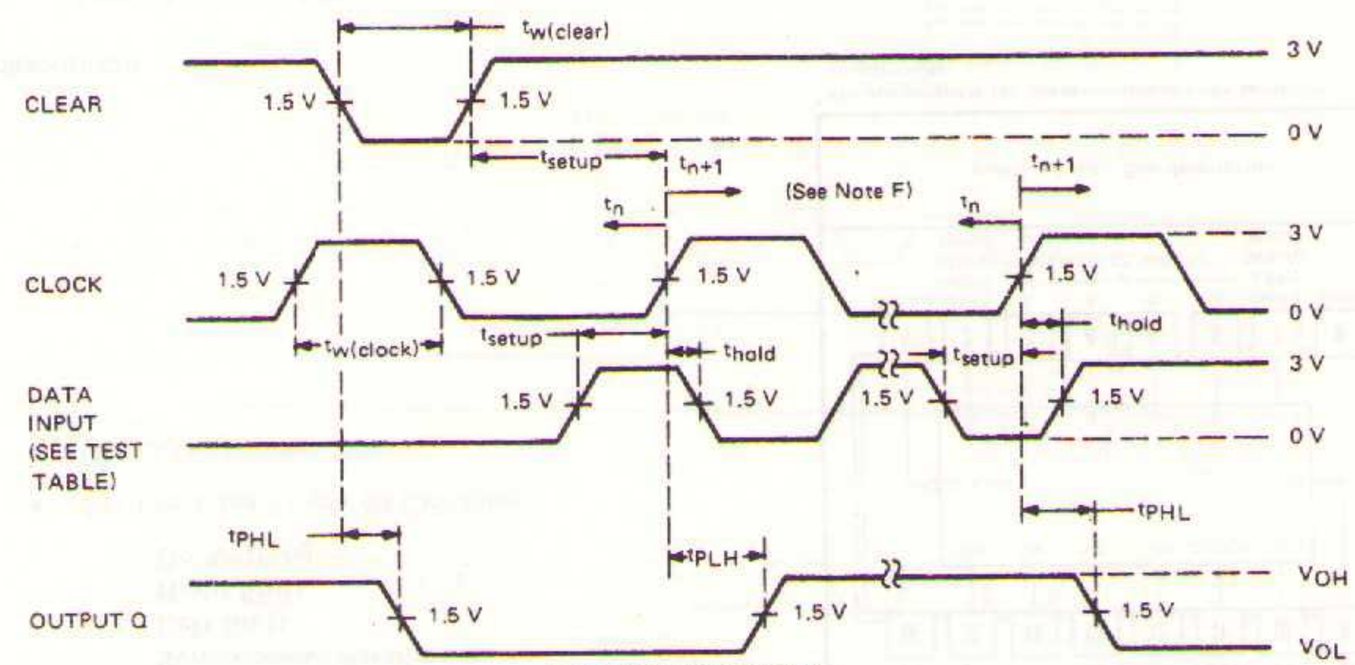
PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST

TEST TABLE FOR SYNCHRONOUS INPUTS

DATA INPUT FOR TEST	S1	S0	OUTPUT TESTED (SEE NOTE E)
A	4.5 V	4.5 V	Q_A at t_{n+1}
B	4.5 V	4.5 V	Q_B at t_{n+1}
C	4.5 V	4.5 V	Q_C at t_{n+1}
D	4.5 V	4.5 V	Q_D at t_{n+1}
L Serial Input	4.5 V	0 V	Q_A at t_{n+4}
R Serial Input	0 V	4.5 V	Q_D at t_{n+4}



VOLTAGE WAVEFORMS

NOTES A. The clock pulse has the following characteristics: $t_{w(clock)} \geq$ 20 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq$ 20 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L includes probe and jig capacitance.

C. All diodes are 1N3064.

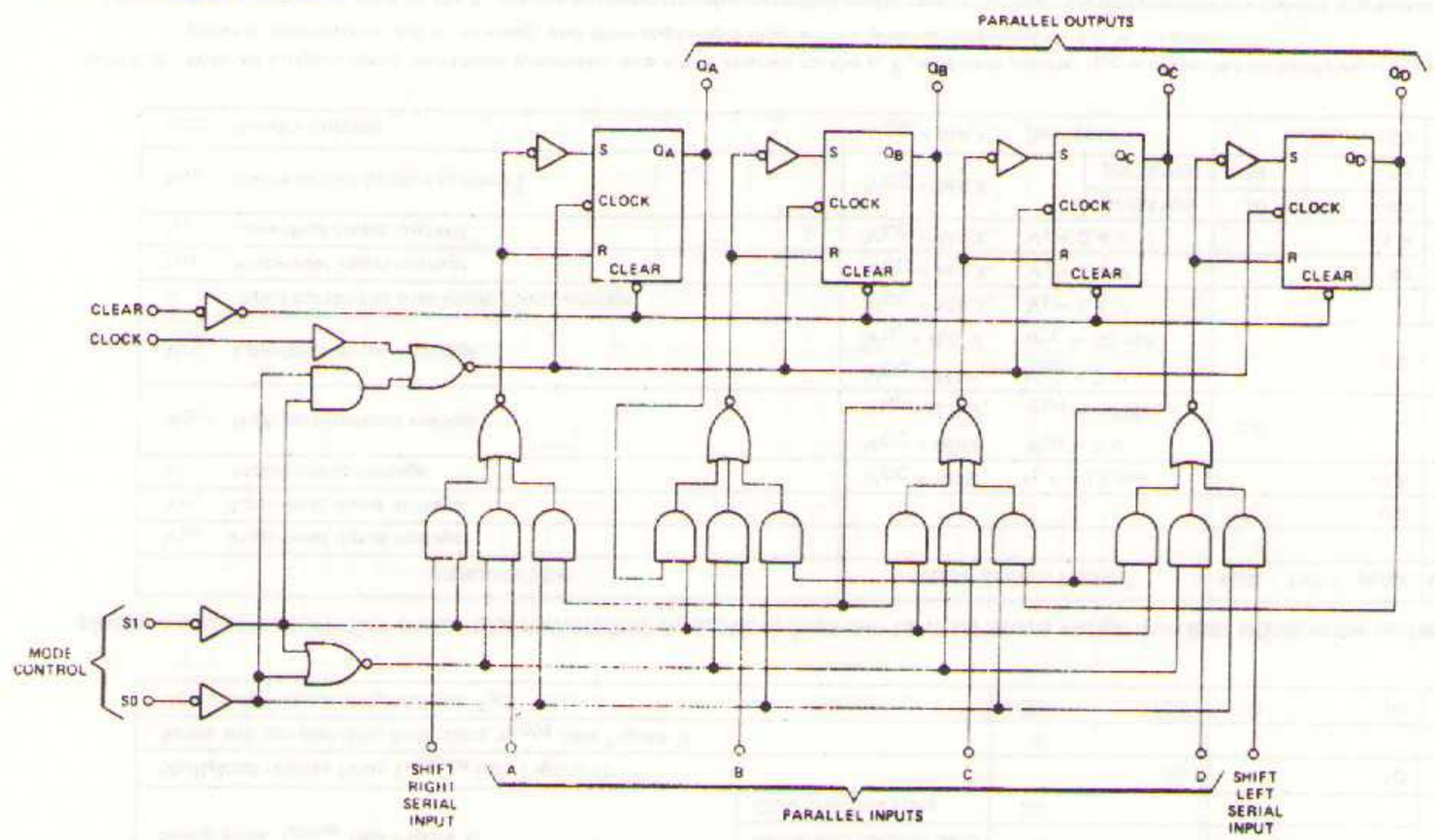
D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

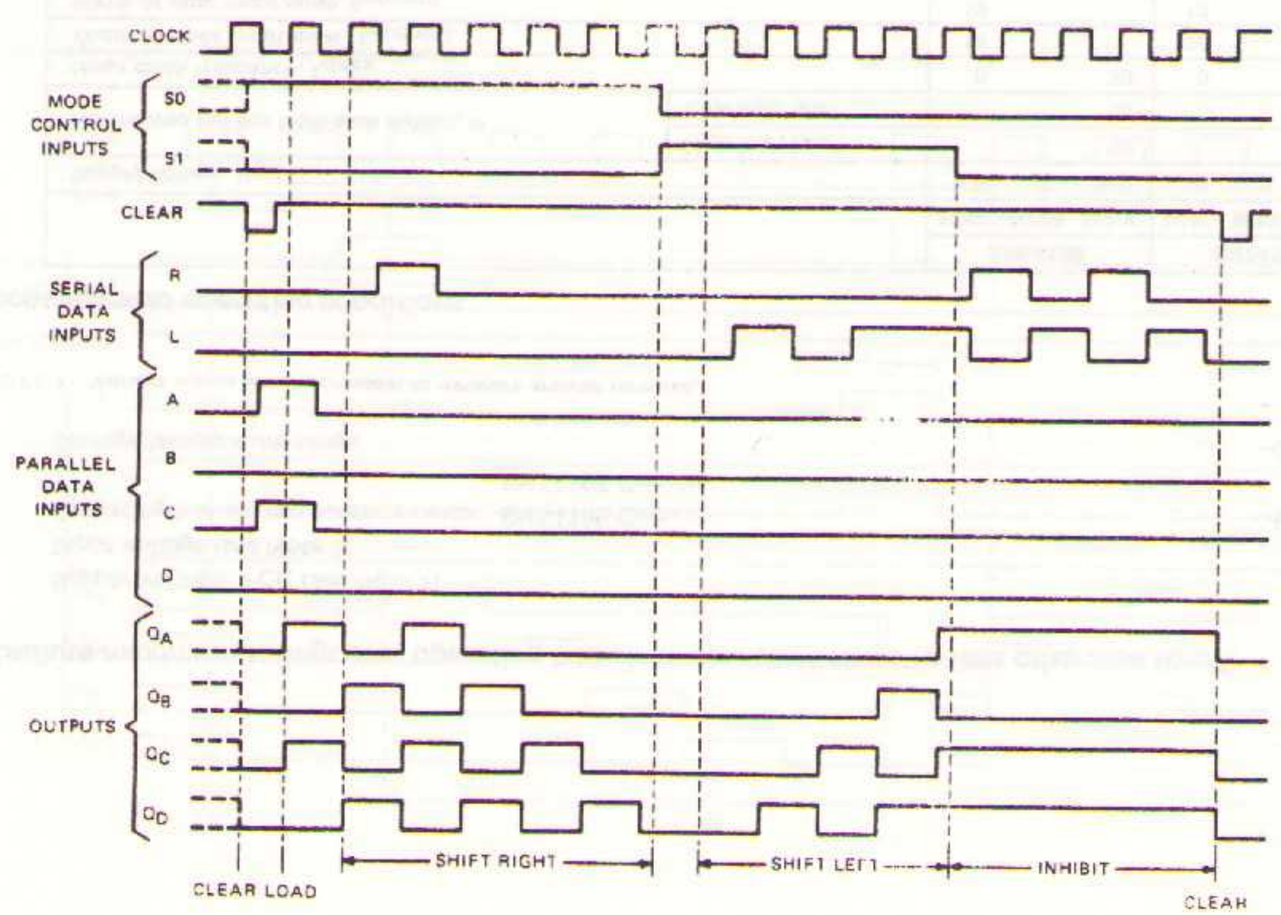
F. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

FIGURE 1–SWITCHING TIMES

functional block diagram

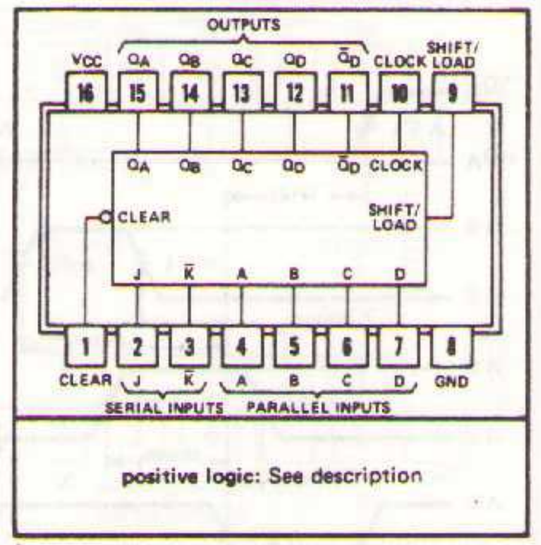


typical clear, load, right-shift, left-shift, inhibit, and clear sequences



- Synchronous Parallel Load
- Positive Edge-Triggered Clocking
- Parallel Inputs and Outputs from Each Flip-Flop
- Direct Overriding Clear
- J and $\overline{K}$ Inputs to First Stage
- Complementary Outputs from Last Stage

J OR N DUAL-IN-LINE
OR W FLAT PACKAGE (TOP VIEW)†



†Pin assignments for these circuits are the same for all packages.

description

These 4-bit registers feature parallel inputs, parallel outputs, J-$\overline{K}$ serial inputs, shift/load control input, and a direct overriding clear. The registers have two modes of operation:

Parallel (Broadside) Load

Shift (In direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking the shift/load control input low. The data is loaded into the associated flip-flop and appears at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shifting is accomplished synchronously when the shift/load control input is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the truth table.

These shift registers are fully compatible with most other TTL and DTL families. All inputs are buffered to lower the drive requirements to one normalized Series 54/74 load, including the clock input. Maximum input clock frequency is typically 39 megahertz and power dissipation is typically 195 milliwatts. The SN54195 is characterized for operation over the full military temperature range of −55°C to 125°C; the SN74195 is characterized for operation from 0°C to 70°C.

TRUTH TABLE

Inputs at t_n		Outputs at t_{n+1}				
J	$\overline{K}$	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	H	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
L	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	L	$\overline{Q}_{An}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

H = high level, L = low level

NOTES: A. t_n = bit time before clock pulse
B. t_{n+1} = bit time after clock pulse
C. Q_{An} = state of Q_A at t_n

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Operating free-air temperature range: SN54195 Circuits	−55°C to 125°C
SN74195 Circuits	0°C to 70°C
Storage temperature range	−65°C to 150°C

NOTE 1: Voltage values are with respect to network ground terminal.

recommended operating conditions

		SN54195			SN74195			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N	High logic level			20			20	
	Low logic level			10			10	
Input clock frequency, f_{clock}		0		30	0		30	MHz
Width of clock input pulse, $t_{w(clock)}$		16			16			ns
Width of clear input pulse, $t_{w(clear)}$		12			12			ns
Setup time, t_{setup} (see Figure 1)	Shift/load	25			25			ns
	Serial and parallel data	15			15			
	Clear inactive-state	25			25			
Shift/load release time, $t_{release}$ (see Figure 1)				10			10	ns
Serial and parallel data hold time, t_{hold} (see Figure 1)		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
I_I	Input clamp voltage	V_{CC} = MIN, I_I = −12 mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA				0.4	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V				40	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−1.6	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	SN54195	−20		−57	mA
			SN74195	−18		−57	
I_{CC}	Supply current	V_{CC} = MAX, See Note 2			39	63	mA

NOTE 2: With all outputs open, shift/load grounded, and 4.5 V applied to the J, $\overline{K}$, and data inputs, I_{CC} is measured by applying a momentary ground, followed by 4.5 V, to clear, and then applying a momentary ground, followed by 4.5 V, to clock.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

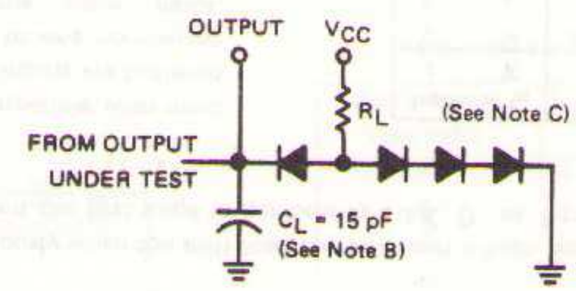
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

§Not more than one output should be shorted at a time.

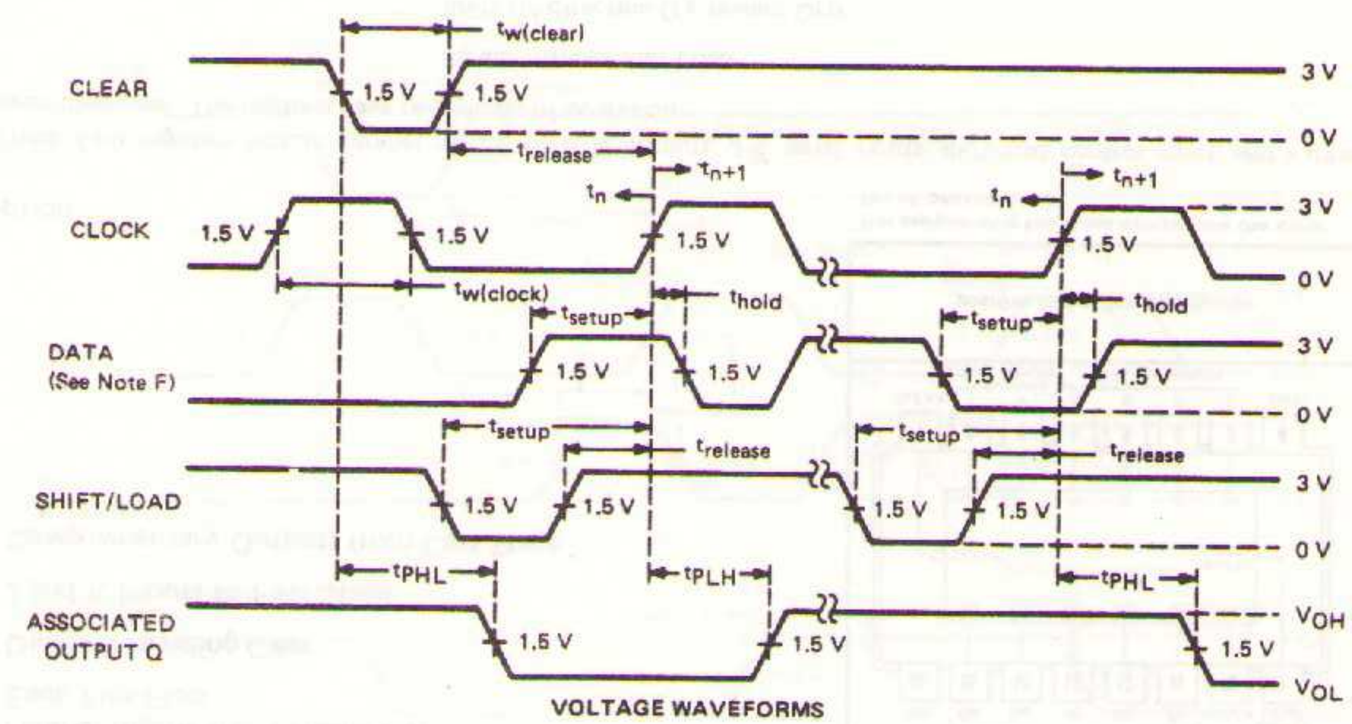
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}	Maximum input clock frequency	C_L = 15 pF, R_L = 400 Ω, See Figure 1	30	39		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			19	30	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock		6	14	22	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		7	17	26	ns

PARAMETER MEASUREMENT INFORMATION



LOAD FOR OUTPUT UNDER TEST



VOLTAGE WAVEFORMS

NOTES: A. The clock pulse has the following characteristics: $t_{w(clock)} \geq$ 16 ns and PRR = 1 MHz. The clear pulse has the following characteristics: $t_{w(clear)} \geq$ 12 ns and t_{hold} = 0 ns. When testing f_{max}, vary the clock PRR.

B. C_L inlcudes probe and jig capacitance.

C. All diodes are 1N3064.

D. A clear pulse is applied prior to each test.

E. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1}. Proper shifting of data is verified at t_{n+4} with a functional test.

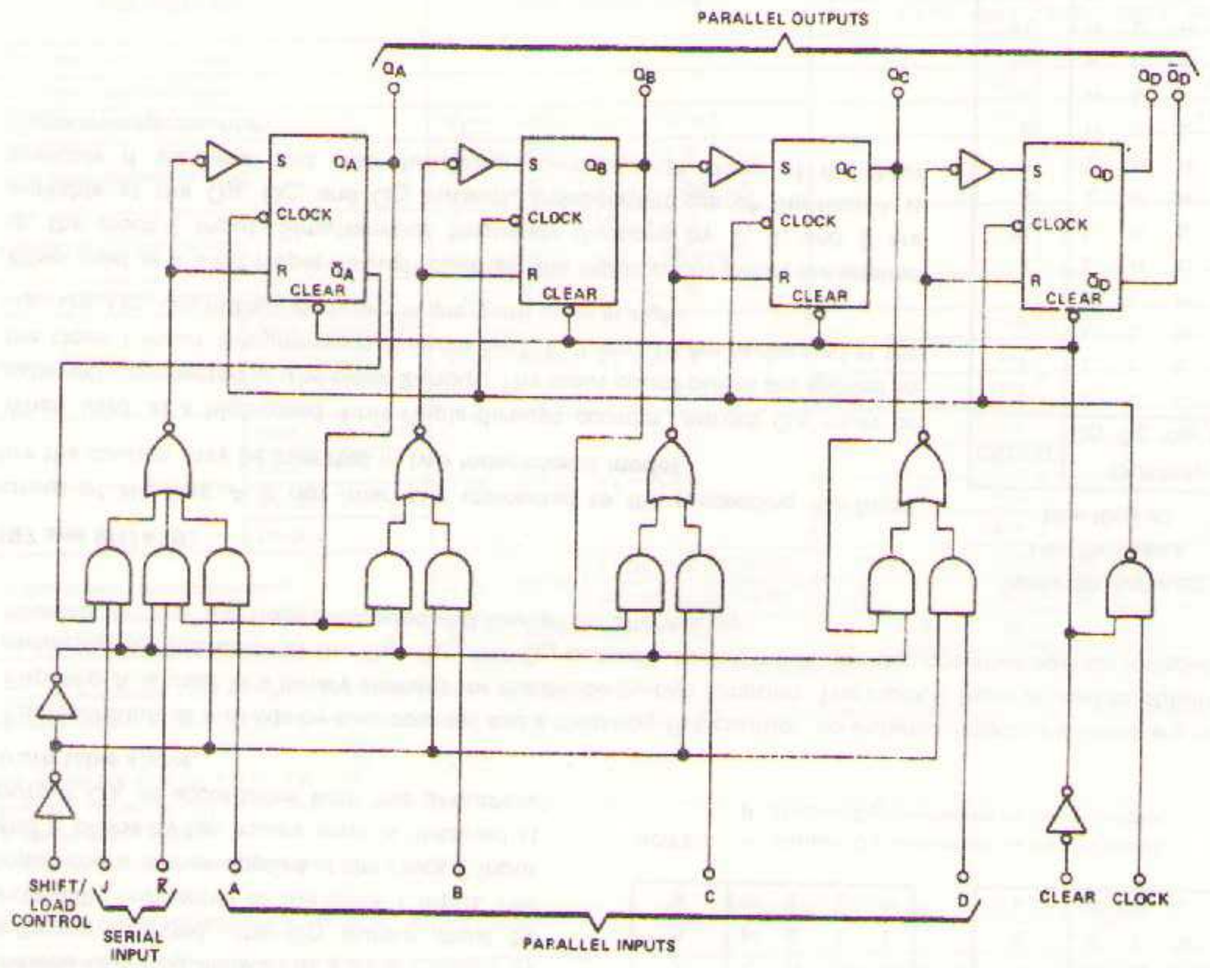
F. J and $\overline{K}$ inputs are tested the same as data A, B, C, and D inputs except that shift/load input remains high.

G. t_n = bit time before clocking transition.
t_{n+1} = bit time after one clocking transition.
t_{n+4} = bit time after four clocking transitions.

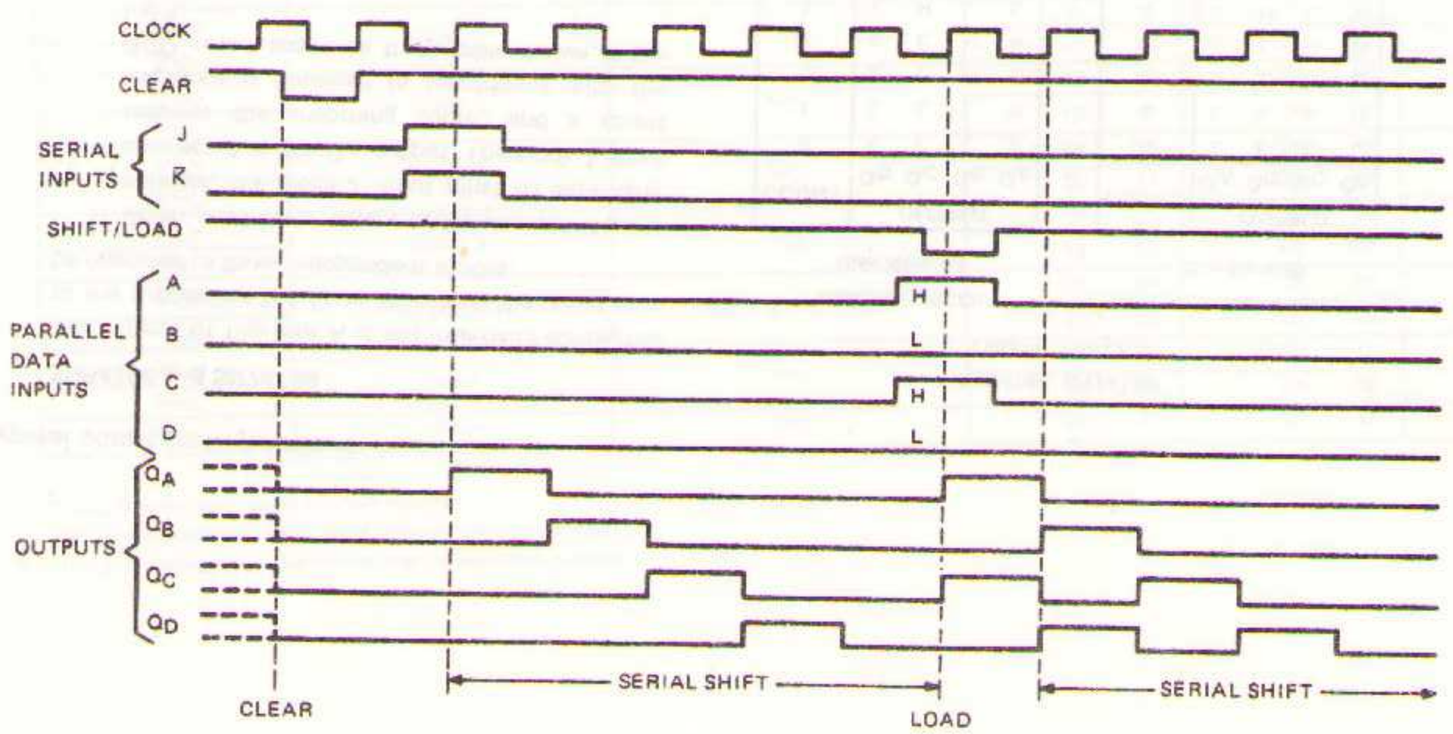
FIGURE 1—SWITCHING TIMES

CIRCUIT TYPES SN54196, SN54197, SN74196, SN74197
BULLETIN NO. DL-S 7111369, OCTOBER 1970
REVISED JANUARY 1971

functional block diagram

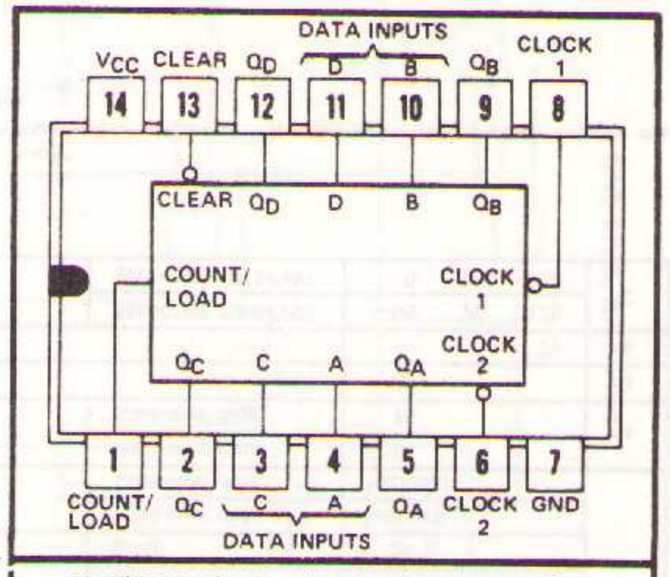


typical clear, shift, and load sequences



- Performs BCD, Bi-Quinary, or Binary Counting
- Fully Programmable
- Fully Independent Clear Input
- Guaranteed to Count at Input Frequencies from 0 to 50 MHz
- Input Clamping Diodes Simplify System Design
- Output Q_A Will Drive Clock-2 Input Plus Ten Series 54/74 Loads

J OR N DUAL-IN-LINE OR
W FLAT PACKAGE (TOP VIEW)†



asynchronous input: Low input to clear sets Q_A, Q_B, Q_C and Q_D low.

†Pin assignments for these circuits are the same for all packages.

description

These high-speed monolithic counters consist of four d-c coupled, master-slave flip-flops which are internally interconnected to provide either a divide-by-two and a divide-by-five counter (SN54196, SN74196) or a divide-by-two and a divide-by-eight counter (SN54197, SN74197). These four counters are fully programmable; that is, the outputs may be preset to any state by placing a low on the count/load input and entering the desired data at the data inputs. The outputs will change to agree with the data inputs independent of the state of the clocks.

These counters may also be used as 4-bit latches by using the count/load input as the strobe and entering data at the data inputs. The outputs will directly follow the data inputs when the count/load is low, but will remain unchanged when the count/load is high and the clock inputs are inactive.

These high-speed counters will accept count frequencies of 0 to 50 megahertz at the clock-1 input and 0 to 25 megahertz at the clock-2 input. During the count operation, transfer of information to the ouputs occurs on the negative-going edge of the clock pulse. These counters feature a direct clear which, when taken low, sets all outputs low regardless of the states of the clocks.

All inputs are diode-clamped to minimize transmission-line effects and simplify system design. These circuits are compatible with most TTL and DTL logic families. Typical power dissipation is 240 milliwatts. The SN54196 and SN54197 circuits are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74197 and SN74197 circuits are characterized for operation from 0°C to 70°C.

typical count configurations

SN54196 and SN74196

The output of flip-flop A is not internally connected to the succeeding flip-flops; therefore, the count may be operated in three independent modes:

1. When used as a binary-coded-decimal decade counter, the clock-2 input must be externally connected to the Q_A output. The clock-1 input receives the incoming count, and a count sequence is obtained in accordance with the BCD count sequence truth table shown at the right.
2. If a symmetrical divide-by-ten count is desired for frequency synthesizers (or other applications requiring division of a binary count by a power of ten), the Q_D output must be externally connected to the clock-1 input. The input count is then applied at the clock-2 input and a divide-by-ten square wave is obtained at output Q_A in accordance with the bi-quinary truth table above.
3. For operation as a divide-by-two counter and a divide-by-five counter, no external interconnections are required. Flip-flop A is used as a binary element for the divide-by-two function. The clock-2 input is used to obtain binary divide-by-five operation at the Q_B, Q_C, and Q_D outputs. In this mode, the two counters operate independently; however, all four flip-flops are loaded and cleared simultaneously.

SN54196, SN74196
TRUTH TABLES

DECADE (BCD)
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY (5-2)
(See Note B)

COUNT	OUTPUT Q_A	Q_D	Q_C	Q_B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

NOTES: A. Output Q_A connected to clock-2 input.
B. Output Q_D connected to clock-1 input.

SN54197 and SN74197

The output of flip-flop A is not internally connected to the succeeding flip-flops, therefore the counter may be operated in two independent modes:

1. When used as a high-speed 4-bit ripple-through counter, output Q_A must be externally connected to the clock-2 input. The input count pulses are applied to the clock-1 input. Simultaneous divisions by 2, 4, 8, and 16 are performed at the Q_A, Q_B, Q_C, Q_D output as shown in the truth table at right.
2. When used as a 3-bit ripple-through counter, the input count pulses are applied to the clock-2 input. Simultaneous frequency divisions by 2, 4, and 8 are available at the Q_B, Q_C, and Q_D outputs. Independent use of flip-flop A is available if the load and clear functions coincide with those of the 3-bit ripple-through counter.

SN54197, SN74197
TRUTH TABLE
(See Note A)

COUNT	OUTPUT Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE A: Output Q_A connected to clock-2 input.

absolute maximum ratings (over operating free-air temperature range unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range:	SN54196, SN54197 Circuits	−55°C to 125°C
	SN74196, SN74197 Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter transistor. For this circuit, this rating applies between the clear and count/load inputs.

recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	SN54196, SN54197	4.5	5	5.5	V
	SN74196, SN74197	4.75	5	5.25	
Normalized fan-out from each output, N	High logic level			20	
	Low logic level			10	
Count frequency (see Figure 1)	Clock-1 input	0		50	MHz
	Clock-2 input	0		25	
Pulse width, t_w (see Figure 1)	Clock-1 input	10			ns
	Clock-2 input	20			
	Clear	15			
	Load	20			
Input hold time, t_{hold} (see Figure 1)	High-level data	$t_{w(load)}$			
	Low-level data	$t_{w(load)}$			
Input setup time, t_{setup} (see Figure 1)	High-level data	10			ns
	Low-level data	15			
Count enable time, t_{enable} (see Note 3 and Figure 1)		20			ns
Clock input pulse fall time, t_f (see Figure 1)				75	ns
Operating free-air temperature range, T_A	SN54196, SN54197	−55	25	125	°C
	SN74196, SN74197	0	25	70	

NOTE 3: Count enable time is the interval immediately preceding the negative-going edge of the clock pulse during which interval the count/load and clear inputs must be both high to ensure counting.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS†		SN54196, SN74196 MIN	SN54196, SN74196 TYP‡	SN54196, SN74196 MAX	SN54197, SN74197 MIN	SN54197, SN74197 TYP‡	SN54197, SN74197 MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.8			0.8	V
V_I	Input clamp voltage		V_{CC} = MAX, I_I = −12 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OH} = −800 μA		2.4			2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = 16 mA¶				0.4			0.4	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5 V				1			1	mA
I_{IH}	High-level input current	data, count/load	V_{CC} = MAX, V_I = 2.4 V				40			40	μA
		clear, clock 1					80			80	
		clock 2					120			80	
I_{IL}	Low-level input current	data, count/load	V_{CC} = MAX, V_I = 0.4 V				−1.6			−1.6	mA
		clear					−3.2			−3.2	
		clock 1					−4.8			−4.8	
		clock 2					−6.4			−3.2	
I_{OS}	Short-circuit output current§		V_{CC} = MAX	SN54196, SN54197	−20		−57	−20		−57	mA
				SN74196, SN74197	−18		−57	−18		−57	
I_{CC}	Supply current		V_{CC} = MAX, See Note 4			48	59		48	59	mA

NOTE 4: I_{CC} is measured with all inputs grounded and all outputs open.

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.

‡All typical values are at V_{CC} = 5 V, T_A = 25°C.

¶Q_A outputs are tested at I_{OL} = 16 mA plus the limit value of I_{IL} for the clock-2 input. This permits driving the clock-2 input while fanning out to 10 Series 54/74 loads.

§Not more than one output should be shorted at a time.

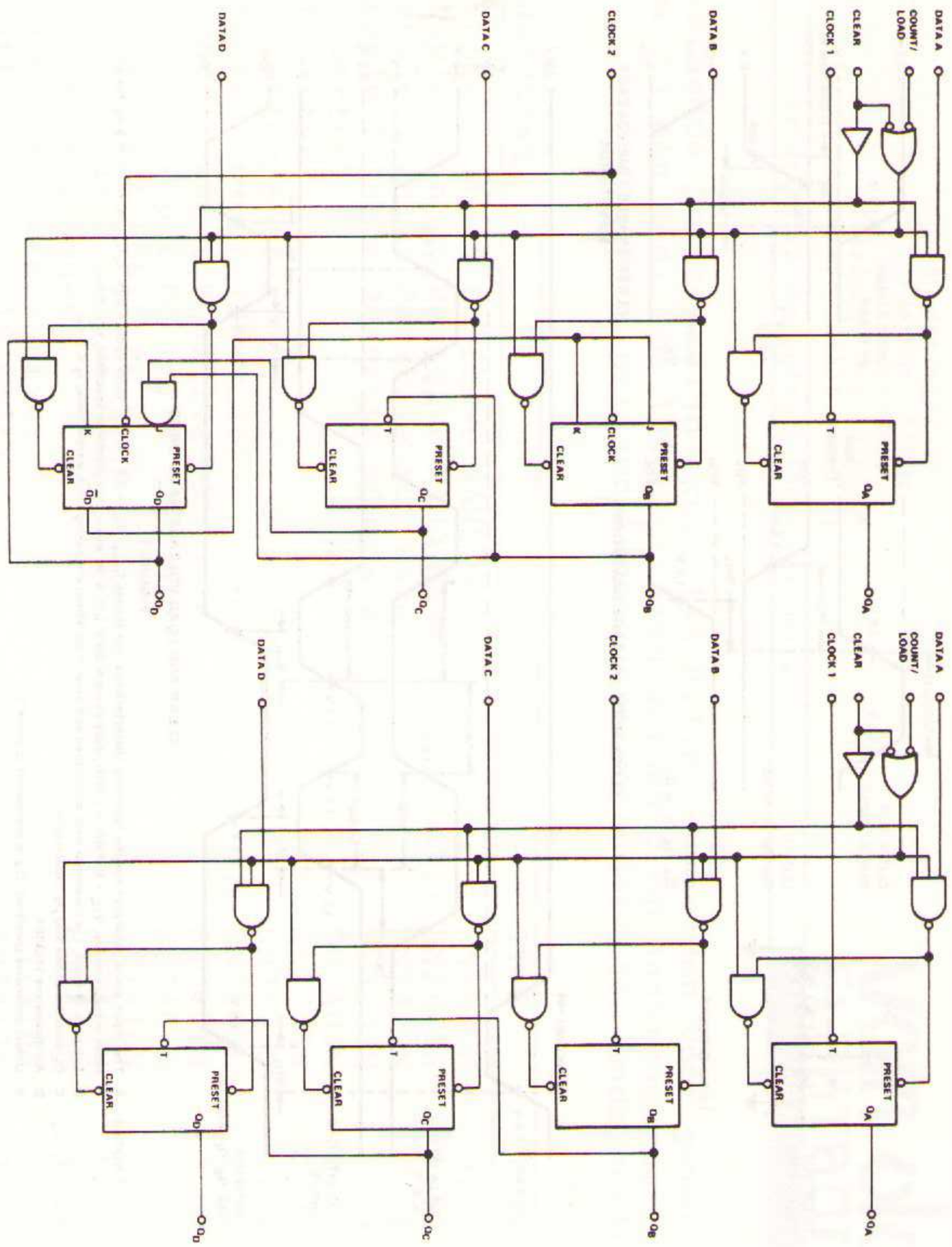
switching characteristics, V_{CC} = 5 V, R_L = 400 Ω, C_L = 15 pF, T_A = 25°C, N = 10, see figure 1

PARAMETER◇	FROM (INPUT)	TO (OUTPUT)	SN54196, SN74196 MIN	SN54196, SN74196 TYP	SN54196, SN74196 MAX	SN54197, SN74197 MIN	SN54197, SN74197 TYP	SN54197, SN74197 MAX	UNIT
f_{max}			50	70		50	70		MHz
t_{PLH}	Clock 1	Q_A		7	12		7	12	ns
t_{PHL}				10	15		10	15	
t_{PLH}	Clock 2	Q_B		12	18		12	18	ns
t_{PHL}				14	21		14	21	
t_{PLH}	Clock 2	Q_C		24	36		24	36	ns
t_{PHL}				28	42		28	42	
t_{PLH}	Clock 2	Q_D		14	21		36	54	ns
t_{PHL}				12	18		42	63	
t_{PLH}	A, B, C, D	Q_A, Q_B, Q_C, Q_D		16	24		16	24	ns
t_{PHL}				25	38		25	38	
t_{PLH}	Load	Any		22	33		22	33	ns
t_{PHL}				24	36		24	36	
t_{PHL}	Clear	Any		25	37		25	37	ns

◇f_{max} is maximum input count frequency

t_{PLH} is propagation delay time, low-to-high-level output

t_{PHL} is propagation delay time, high-to-low-level output



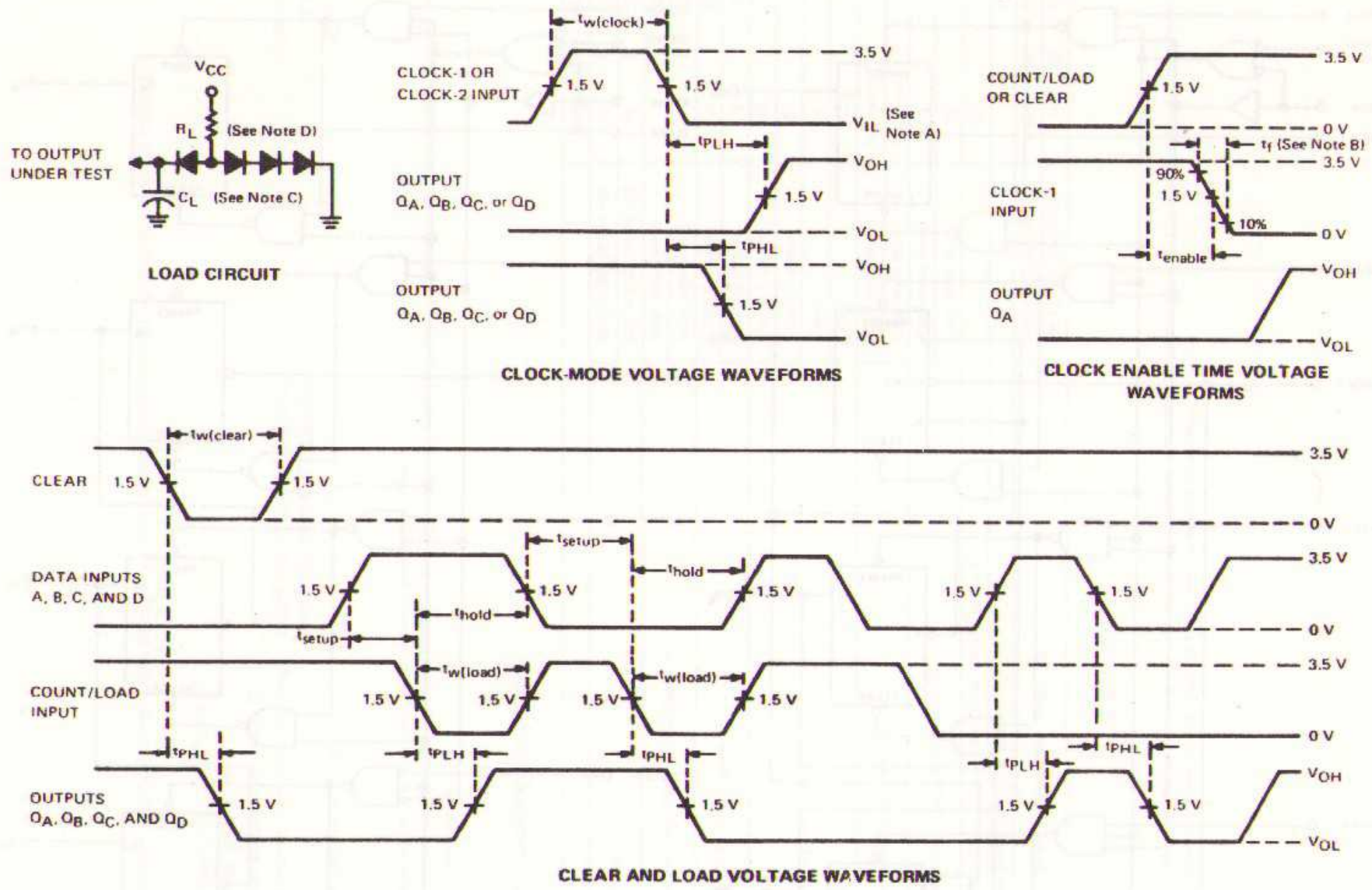


FIGURE 1

NOTES: A. The input pulse generator has the following characteristics: for testing f_{max}, $V_{IL} = 0.3 \pm 0.1$ V, duty cycle = 50%, $t_r < 5$ ns, and $t_f < 5$ ns; for all other measurements, $V_{IL} = 0$, PRR < 1 MHz, duty cycle < 50%, $t_r < 5$ ns, and unless otherwise specified, $t_f < 5$ ns.

B. Fall time of clock 1 is measured with count/load and clear high. When measuring clock enable time, $t_f < 5$ ns.

C. C_L includes probe and jig capacitance.

D. All diodes are 1N3064.

E. Unless otherwise specified, Q_A is connected to clock 2.

IC VOETEN

Voor het monteren van Uw geïntegreerde schakelingen op experimenteerkaarten danwel definitieve prints is een uitgebreid programma voeten voor 14 pens, 16 pens en 24 pens IC's beschikbaar. Op dit punt kan onze Handelmaatschappij U diverse uitvoeringen aanbieden, waaruit wij onder andere noemen:

Molex IC terminals: deze terminals, staande op een 0,1" raster, worden aan band geleverd en kunnen op de drager afgeknipt worden in elke gewenste kwantiteit. Hierdoor is een geringe voorraadinvestering voldoende om een bijzonder universeel geheel te verkrijgen. Voor deze terminals zijn de onderstaande prijzen van toepassing:

aan band van 100 stuks bij afname van 1-499 terminals	f 0,07
aan band van 100 stuks bij afname van 500-999 terminals	f 0,061
aan band van 1000 stuks bij afname van 1000-4999 terminals	0,0525
aan band van 1000 stuks bij afname van 5000-9999 terminals	0,0425

voor een steviger op de print montage zijn van Molex ook plastic stukjes leverbaar om 7 of 8 pennen naast elkaar in te steken teneinde een betere mechanische stevigheid te creëren. Deze kosten per set van 2 plastic stukjes:

voor de 7 pens uitvoering	f 0,20
voor de 8 pens uitvoering	f 0,25

BOVENSTAANDE prijzen zijn alle excl. 14% BTW en kunnen veranderd worden.

Voor de vele andere typen voeten kunt U het best kontakt opnemen met onze afdeling verkoop, waar onze technici U gaarne nader zullen informeren.

B.V. TECHNISCHE HANDELMAATSCHAPPIJ

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Postbus 450
Rotterdam-3004
Telefoon: 010 - 670022*
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Onderstaande prijzen zijn excl. 14% B.T.W. en gelden voor gemengde (!) afname in één keer. De 100up prijzen worden U op aanvraag gaarne verstrekt. Onderstaande prijzen kunnen aan veranderingen onderhevig zijn.

OMSCHRIJVING	TYPE	1-24	25-99
Quadruple 2-Input Positive NAND Gate	SN7400N	1,58	1,39
Quadruple 2-Input Positive NAND Gate (Open Coll.)	SN7401N	1,58	1,39
Quadruple 2-Input Positive NOR Gate	SN7402N	1,58	1,39
Quadruple 2-Input Positive NOR Gate (Open Coll.)	SN7403N	1,58	1,39
Hex Inverter	SN7404N	2,21	1,94
Hex Inverter	SN7405N	2,21	1,94
Hex Inverter/Buffer/Driver (30 volt)	SN7406N	4,28	3,76
Hex Buffer/Driver (30 volt)	SN7407N	4,28	3,76
Quadruple 2-Input Positive AND Gate	SN7408N	2,07	1,82
Quadruple 2-Input Positive AND Gate	SN7409N	2,07	1,82
Triple 3-Input Positive NAND Gate	SN7410N	1,58	1,39
Triple 3-Input Positive NAND Gate with OC	SN7412N	1,58	1,39
Dual Schmitt Trigger	SN7413N	4,28	3,76
Hex Inverter/Buffer/Driver (15 volt)	SN7416N	3,15	2,77
Hex Buffer/Driver (15 volt)	SN7417N	3,15	2,77
Dual 4-Input Positive NAND Gate	SN7420N	1,58	1,39
Dual 4-Input Positive NOR Gate (Expandable)	SN7423N	2,39	2,10
Dual 4-Input Positive NOR Gate	SN7425N	2,39	2,10
Quadruple 2-Input Positive NAND Gate (30 volt)	SN7426N	2,39	2,10
Triple 3-Input Positive NOR Gate	SN7427N	2,39	2,10
Quad 2 NOR Power	SN7428N	3,24	2,85
8-Input Positive NAND Gate	SN7430N	1,58	1,39
Quad 2-Input Positive OR Gate	SN7432N	2,39	2,10
Quadruple 2-Input Positive NAND Buffer	SN7437N	3,06	2,69
As type SN7437N (with Open Collector)	SN7438N	3,06	2,69
Dual 4-Input Positive NAND Buffer	SN7440N	1,98	1,74
BCD-to-Decimal Decoder	SN7442N	8,10	7,13
Excess-3-to-Decimal Decoder	SN7443N	8,55	7,52
Excess-3 Gray-to-Decimal Decoder	SN7444N	8,55	7,52
BCD-to-Decimal Decoder/Driver (80 mA sink)	SN7445N	15,30	13,46
BCD-to-Seven Segment Decoder/Driver (20mA sink)	SN7446AN	12,96	11,40
BCD-to-Seven Segment Decoder/Driver (20mA sink)	SN7447AN	9,45	8,32
BCD-to-Seven Segment Decoder/Driver (10mA sink)	SN7448N	12,96	11,40
Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate	SN7450N	1,58	1,39
Dual 2-Wide 2-Input AND-OR-INVERT Gate	SN7451N	1,58	1,39
Expandable 4-Wide 2-Input AND-OR-INVERT Gate	SN7453N	1,58	1,39
4-Wide 2-Input AND-OR-INVERT Gate	SN7454N	1,58	1,39
Dual 4-Input Expander	SN7460N	1,58	1,39
J-K Flip-Flop	SN7470N	3,45	3,04
J-K Master-Slave Flip-Flop	SN7472N	2,43	2,14
Dual J-K Master-Slave Flip-Flop	SN7473N	3,87	3,41
Dual D-Type Edge-Triggered Flip-Flop	SN7474N	3,38	2,97
Quadruple Bistable Latch	SN7475N	5,58	4,91
Dual J-K Master-Slave Flip-Flop with Preset/Clear	SN7476N	4,14	3,64
Gated Full Adder	SN7480N	4,95	4,36
16-Bit Active Element Memory	SN7481N	9,00	7,92
2-Bit Binary Full Adder	SN7482N	7,20	6,34
4-Bit Binary Full Adder	SN7483N	10,13	8,91

OMSCHRIJVING	TYPE	1-24	25-99
16-Bit Active Element Memory (Gated Write Inputs)	SN7484N	9,68	8,51
4-Bit Magnitude Comparator	SN7485N	14,85	13,07
Quadruple 2-Input Exclusive OR Gate	SN7486N	2,79	2,46
64-Bit Read/Write Memory	SN7489N	46,00	40,48
Decade Counter	SN7490N	5,85	5,15
8-Bit Shift Register	SN7491AN	8,91	7,84
Devide-by-Twelve Counter	SN7492N	5,85	5,15
4-Bit Binary Counter	SN7493N	5,85	5,15
4-Bit Shift Register	SN7494N	8,10	7,13
4-Bit Right/Left Shift Register	SN7495N	6,35	5,58
5-Bit Shift Register	SN7496N	10,35	9,10
Synchronous Rate Multipliers	SN7497N	29,25	25,74
Dual Quadruple Bistable Latch	SN74100N	11,81	10,40
Gated J-K Master-Slave Flip-Flops	SN74104N	5,58	4,91
Gated J-K Master-Slave Flip-Flops	SN74105N	5,58	4,91
Dual J-K Master-Slave Flip-Flops	SN74107N	3,87	3,41
High Speed J-K Flip-Flops	SN74110N	5,67	4,99
Dual J-K M-S F-F with Data Lockout	SN74111N	9,72	8,55
6-Bit Latch	SN74118N	10,58	9,31
6-Bit Latch	SN74119N	13,73	12,08
Monostable	SN74121N	4,45	3,92
Retriggable O.S. with Clear	SN74122N	5,98	5,26
Retriggable Monostable Multivibrators with Clear	SN74123N	11,95	10,52
Quadruple 2-Input Schmitt Trigger	SN74132N	8,19	7,21
BCD-to-Decimal Decoder/Driver	SN74141AN	8,51	7,48
BCD-to-Decimal Decoder/Driver (80mA sink)	SN74145N	12,81	11,28
16-Bits Data Selector	SN74150N	16,20	14,26
8-Bits Data Selector (with Strobe)	SN74151N	7,65	6,73
Dual 4-Line-to-1-Line Data Selector/Multiplexer	SN74153N	6,75	5,94
4-Line-to-16-Line Decoder/Demultiplexer	SN74154N	14,40	12,67
Dual 2-to-4-Line Decoder/Demultiplexer	SN74155N	7,65	6,73
Dual 2-to-4-Line Decoder/Demultiplexer	SN74156N	7,65	6,73
Dual 2-to-4-Line Decoder/Demultiplexer	SN74157N	9,00	7,92
Synchronous 4-Bit Counters	SN74160N	13,60	11,97
Synchronous 4-Bit Counters	SN74161N	13,60	11,97
Synchronous 4-Bit Counters	SN74162N	13,60	11,97
Synchronous 4-Bit Counters	SN74163N	13,60	11,97
8-Bit Parallel-Out Serial Shift Register	SN74164N	16,56	14,58
Parallel-Load 8-Bit Shift Register	SN74165N	16,56	14,58
Synchroon Parallel-Load 8-Bit Shift Register	SN74166N	16,56	14,58
Synchronous Rate Multipliers	SN74167N	26,45	23,28
4-by-4 Register File	SN74170N	18,81	16,56
Hex D-Type Flip-Flops with Clear	SN74174N	13,05	11,48
Quad D-Type Flip-Flops with Clear	SN74175N	9,90	8,71
Decade Counter 25 MHz	SN74176N	15,30	13,46
Binary Counter 25 MHz	SN74177N	15,30	13,46
8-Bit Odd/Even Parity Generator/Checker	SN74180N	11,38	10,01
4-Bit Arithmetic Logic Unit	SN74181N	33,75	29,70
Look-Ahead Carry Generator	SN74182N	9,45	8,32
BCD-to-Binary and Binary-to-BCD Converters	SN74184N	23,44	20,63
Binary-BCD-Decoder	SN74185AN	23,44	20,63
Synchroon Decade Up/Down Counter	SN74190N	14,40	12,67
Synchroon 4-Bits Up/Down Counter	SN74191N	14,40	12,67
Synchroon Decade Up/Down Counter	SN74192N	15,75	13,86
Synchroon 4-Bits Up/Down Counter	SN74193N	15,75	13,86
4-Bit Bidirectional Universal Shift Register	SN74194N	15,19	13,37
4-Bit Parallel-Access Shift Register	SN74195N	15,19	13,37
50-MHz Presettable Decade Counter	SN74196N	15,19	13,37
50-MHz Presettable 4-Bit Binary Counter	SN74197N	15,19	13,37
8-Bit Parallel-Access, Left-Shift Right-Shift Reg.	SN74198N	24,30	21,38
8-Bit Parallel-Access Shift Register	SN74199N	21,15	18,61

printproduktie

Sinds januari j.l. is onze Technische Handelsmaatschappij uitgebreid met een afdeling "Printproduktie", welke zich bezig houdt met het vervaardigen van allerhande gedrukte bedradingen in kleine of grote kwantiteiten. Speciaal voor proefprinten is een super-snelle service ingesteld, zodat Uw proefprinten overdag (ongeboord) binnen circa 5 uur nadat deze in ons bezit is gekomen, gereed ligt ter levering, terwijl een geboorde print een één uur langere levertijd heeft. De uiteindelijke levertijd wordt nu slechts nog bepaald door de tijd van toezending van U naar ons bedrijf en v.v.

Ter oriëntatie enkele prijzen voor proefprints bij afname van 1-5 stuks in één bestelling:

–	fotokosten (eenmalig)	f 15,00
–	phenol papier, éénzijdig en ongeboord	f 0,035 per cm^2
–	epoxy, éénzijdig en ongeboord	f 0,055 per cm^2
–	epoxy, dubbelzijdig en ongeboord	f 0,075 per cm^2
–	boringen in phenol papier	f 0,008 per gat
–	boringen in epoxy	f 0,01 per gat

op basis van een goede geplakte tekening!

Bovenstaande prijzen zijn excl. 14% BTW en verzendkosten, terwijl op bovenstaande prijzen tevens onze leveringsvoorwaarden van toepassing zijn.

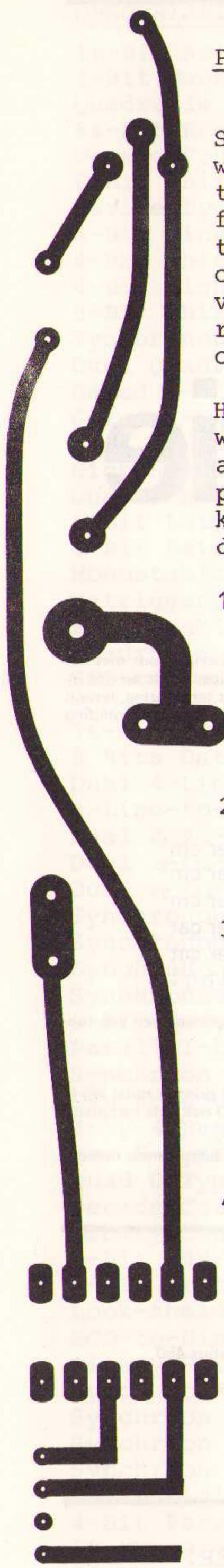
Ook voor grotere series kunnen wij U een scherpe prijs aanbieden: stuurt U gerust eens een fotokopie van één Uwer printen zodat wij U een passende en vrijblijvende offerte kunnen maken voor het door U gewenste aantal. Grotere series kunnen wij voor U ook vele metalleurgische behandelingen geven; onze afd. printproduktie zal U hierover gaarne inlichten (010-670022 toestel 7).

Wilt U onze kwaliteit leren kennen? Stuurt U ons eens Uw volgende proefprint-opdracht zodat wij U hiermee kunnen laten kennis maken!

B.V. Technische Handelsmaatschappij

Spoorsingel 49 (blijdorp-uitgang CS-station), Postbus 450,
Rotterdam-3004, telefoon: 010-670022,
telex: 25336 damel nl, postgirorekening: 29 55 50.

ZIE NAVOLGENDE PAGINA'S HIEROVER!



Proefprintservice

Sinds de oprichting van onze afdeling elektronica zijn wij zelf een grootverbruiker op het gebied van gedrukte bedradingen geweest en -net als U wellicht- geconfronteerd met lange levertijden en slechte afwerkingen, twee belangrijke punten welke ons ertoe hebben aangezet om zelf prints te gaan vervaardigen. Vooral het maken van proefprints is met onze inrichting van de produktieruimte als belangrijk punt in acht genomen, waarvoor dan ook een speciale produktiestraat is samengesteld.

Hierdoor kan nu ook voor U een unieke service geboden worden welke kan resulteren in een snellere service aan Uw relaties. Voor kleine series kunnen wij een produktietijd geven van circa 5 uur na het in het bezit komen van Uw -goede- printtekening. Hiervoor dient wel door U aan de volgende voorwaarden te worden voldaan:

1. de tekening moet geplakt zijn met Brady of Mecanorma op hagelwit papier of plastic folie (verkrijgbaar met makkelijk plakraster!). Telkens ontvangen wij tekeningen met oost-indische inkt; deze zijn doorgaans onbruikbaar doordat deze inktsoort transparant is (houdt U zo'n tekening maar eens in het licht of voor een lamp!).
2. de tekening mag op elke schaal zijn, mits voorzien van een maataanduiding. Hoe groter de tekening is t.o.v. het gewenste eindprodukt, des te beter de uiteindelijk bereikbare kwaliteit is.
3. de prijzen zijn gebaseerd op prints zonder speciale connector-uitsparingen en voor afwerking met een soldeercoating. Andere maten en/of oppervlakte-behandelingen zijn op basis van meerprijs. Met nadruk wijzen wij erop, dat de aan ommezijde (pag. 129) vermelde proefprintprijzen zijn gebaseerd op vierkant of rechthoekig afgewerkte prints zònder speciale uitsparingen in hoeken of op andere plaatsen in de zijkanten of andere gaten dan ronde.
4. tegen meerprijs is voor prints met een connectordeel vergulden over een nikkelcoating mogelijk. Dergelijke prints vallen echter NIET onder de proefprintservice daar dergelijke extra behandeling ca. 20-30 minuten per print extra vergt. De levertijd loopt hierdoor wel uit met circa 1 dag extra. Een richtprijs voor goudkontakten kan niet zonder tekening gegeven worden, daar goud niet tot de goedkoopste metalen behoort en het bepalen van het aan te brengen gewicht van essentieel belang maakt.
5. ook chemische vernikkeling van Uw koperbanen en eilanden kan door ons bedrijf gedaan worden tegen meerprijs. Prijzen op aanvraag na toezending van Uw tekening of een kopie daarvan.

VOOR EEN UITGEBREID PROGRAMMA TEKENMATERIAAL ZIE PAGINA 131.

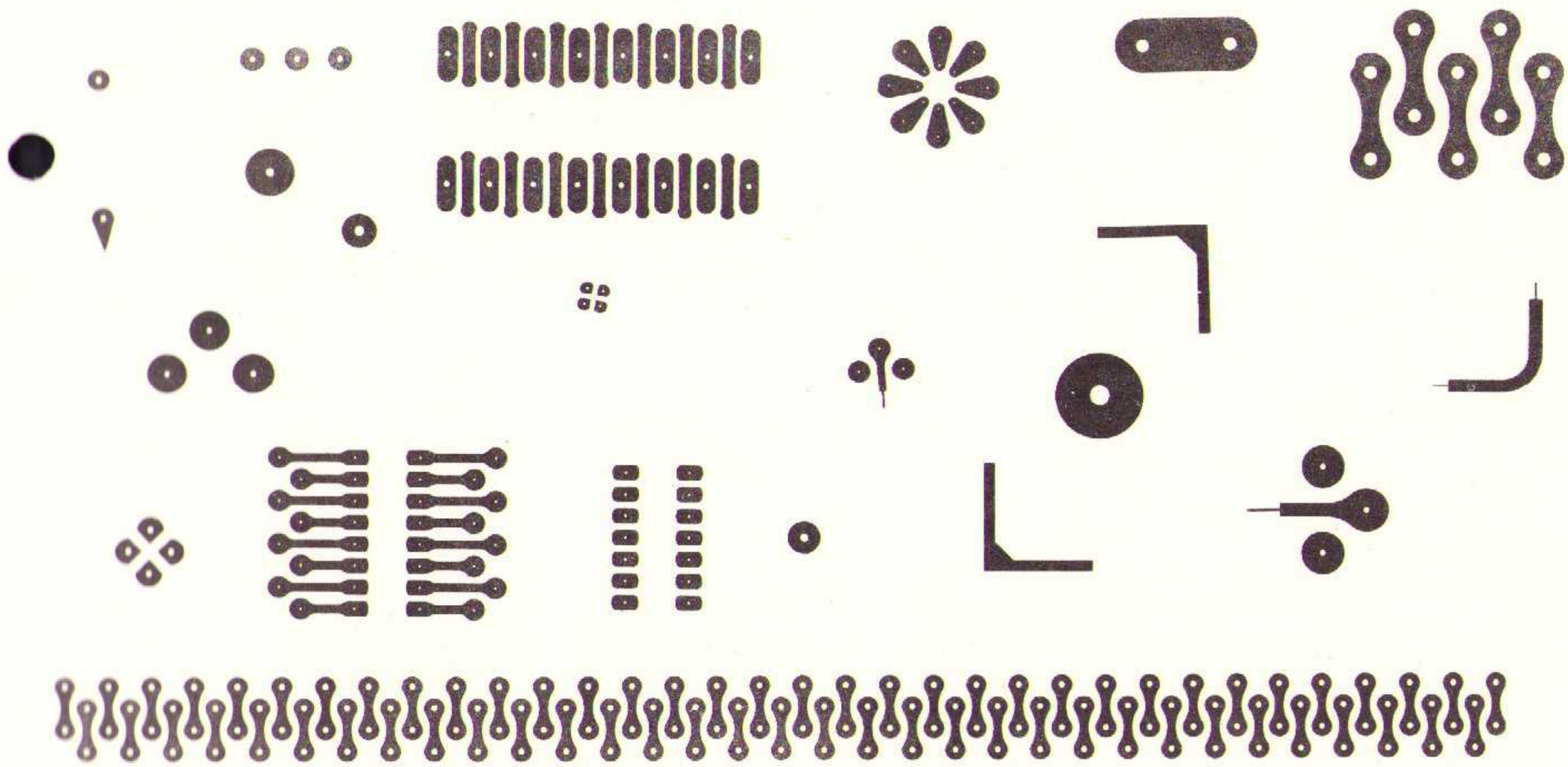
MECANORMA
ELECTRONIC

PRINTTEKENMATERIALEN

Bij deze documentatie is -voor zover het niet verloren is, danwel door derden eruit verwijderd- een monsterstrookje bijgeleverd van 'mecanorma' printplak materialen. Deze materialen bestaan uit een plastic drager met het printsymbool (soldeereiland, ic-soldeereiland, elleboogje, o.i.d.) eronder. Deze reeks materialen vereenvoudigen het vervaardigen van een printtekening drastisch en maken het tot een pleziertje een printtekening te vervaardigen, hoe gecompliceerd of gevarieerd ook. Deze plaksymbolen zijn leverbaar in vele variëteiten en schalen, waarvoor wij U verwijzen naar een -gratis- beschikbare catalogus.

Waardoor onderscheidt zich Mecanorma van andere merken? Mecanorma is een zeer dun materiaal, waardoor het onderdringen van licht op plaatsen, waar koperbaanplaksel en soldeereiland elkaar overlappen, onmogelijk is geworden. Bovendien zijn bijvoorbeeld de IC plaksymbolen op één drager ondergebracht, waardoor deze immer op het juiste raster op de print over komen. De diverse symbolen zijn doorgaans ook nog voorzien van een markeringskruisje om een juiste plaatsing op de print te bewerkstelligen. Ook de grote gevariëerdheid van dit materiaal doet vele naar Mecanorma overstappen. Over het juiste gebruik van printtekenmaterialen komt in een van de komende documentaties een uitgebreid artikel, want velen maken hierbij fouten ten aanzien van het door de fabrikant bedoelde gebruik, waardoor de grote voordelen van een materiaal niet voor 100% worden uitgebuit.

Een beknopt overzicht van de leverbare symbolen hebben wij hieronder opgenomen: zoals wij hierboven reeds stelden is een gratis catalogus -met eventuele monsters indien ze niet meer bij deze documentatie werden aangetroffen- beschikbaar, aan te vragen bij Postbus 450 te Rotterdam-3004.



PRIJZEN EN TYPENUMMERS WORDEN BIJ DE CATALOGUS BIJGEVOEGD EN BINNENKORT OOK IN DEZE DOCUMENTATIE-UITGAVE OPGENOMEN.

Technische documentatie 1972

Op veler verzoek wordt deze voor Europa nog steeds unieke documentatie-uitgave voortgezet, echter in een nieuwe vorm. Met ingang van 1972 wordt op een uitgebreidere manier aandacht besteed aan nieuwe produkten van onze internationaal opererende handelmaatschappij en verkrijgt ook iets meer de vorm van een technische catalogus.

Sinds de eerste uitgaven van deze documentatie is de stuctuur van onze handelmaatschappij gewijzigd, iets wat dient te worden doorgevoerd in onze neven-activiteiten en de interessantheid van deze documentatie ongetwijfeld ten goede gaat komen.

Voor de verlenging van Uw abonnement wordt U binnen enkele dagen na ontvangst van deze documentatie een acceptgiro ten bedrage van *f* 15,= toegezonden. Wij verzoeken U zeer dringend Uw verlenging van het abonnement hiermee te voldoen, daar deze acceptgirokaart ook administratieve gegevens (o.a. Uw abonnementnummer) bevat, welke een juiste verwerking van Uw betaling waarborgen.

De technsiche documentatie van 1972 wordt gepresenteerd als kwartaaluitgave en krijgt ook een nieuw frontaanzicht. In verband met het vertraagd uitkomen van de delen van 1971 wordt de eerste kwartaaluitgave omstreeks juli verwacht.

TECHNISCHE DOCUMENTATIE is een speciale bedrijfsuitgave van

van dam
ELEKTRONICA

en dient om het bedrijfsleven en amateurs in staat te stellen te weten wat de produkten, welke ook oa. bij Van Dam Elektronica verkrijgbaar zijn, technisch zijn en kunnen doen -en, wat wel eens nòg belangrijker is, niet kunnen doen-.

VERLENG UW ABONNEMENT S.V.P. MET DE ACCEPTGIRO EN U VOORKOMT ONJUISTE VERWERKING VAN UW VERLENGING EN VEEL ONGEMAK VOOR U EN ONZE ADMINISTRATIE